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Neural-Based Models of Semiconductor Devices for SPICE Simulator

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Abstract: The paper addresses a simple and fast new approach to implement Artificial Neural Networks (ANN) models for the MOS transistor into SPICE. The proposed approach involves two steps, the modeling phase of the device by NN providing its input/output patterns, and the SPICE implementation process of the resulting model. Using the Taylor series expansion, a neural based small-signal model is derived. The reliability of our approach is validated through simulations of some circuits in DC and small-signal analyses.

Keywords: Artificial Neural Networks, new semiconductor devices, SPICE, Modeling, Taylor series expansion.

INTRODUCTION

Although the MOS (Metal Oxide Semi-conductor) transistor [1-2] is not a recent semi-conductor device, it remains of a potential interest for large-scale Integrated Circuits (IC) due to its electrical properties.

Owing to the rapid changes in semi-conductor technology, development of models to characterize the new transistor behaviors has become a continuous activity and an essential component of the design cycle. Therefore, it is very important for efficient Computer Aided Design (CAD) tools to have good modeling approaches able to predict the device DC and small-signal nonlinear behaviors. These models must be accurate, reliable, easily extracted and have limited computational requirements.

Several SPICE models for the MOS transistor have been reported [1-3]. However, most of them use more than one equation to capture the non-linear MOS behavior under the different operating regions. Since SPICE was written originally for silicon devices only, differences with other material devices, GaAs among others, need to be handled. Hermann et al. [4] showed how it is complex to adapt SPICE models. Existing approaches for transistor modeling are based on lumped equivalent circuits. The equivalent circuit approach involves determination of an equivalent circuit topology and formulation of the circuit elements. Such an approach not only requires experience but also a difficult trial and process.

Recently, ANN have been recognized as a powerful tool for modeling and optimization problems [5-8]. The universal approximation property of ANN [9-10] provides them the ability to learn any arbitrarily nonlinear input-output relationships [11-14] from corresponding measured or simulated data.

Moreover, researches started investigating NN approaches to model transistor DC [15-19], small signal [20-21], and large-signal [22-27] behaviors. Xiuping et al. [28] have proposed an improved microwave active device modeling technique based on the combination of the equivalent circuit and ANN approaches. NN transistor models can be developed even if the device theory/equations are unavailable. Works dealing with the implementation of NN models into SPICE are rare. We mention the reference [29-30] describing the implementation of NN in SPICE as electrical circuits.

We present a NN model for the MOS transistor given by a single mapping function. As the drain current depends of the drain-to-source, V_d and gate-to-source, V_g, bias voltages, it was implemented into SPICE as a voltage-controlled current source. Using the Taylor series expansion, a small signal MOS model is derived.

MATERIALS AND METHODS

Problem statement: DC model: Commonly used NNs structures for black box modelling are Multi-Layer Perceptron (MLP). A MLP with one hidden sigmoid layer is able to model almost any physical function accurately provided that a sufficient number of hidden neurons are available [31-32].

In our study, in the simplest situation, we may consider the MOS transistor as a three-terminal device. The drain current I_d is the predominant nonlinear element in the transistor, which depends, on DC

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behavior, on the drain-to-source, V_d and gate-to-source, V_g, bias voltages. So the terminal voltages V_d and V_g are the neural network input parameters and the drain current I_d is the NN output. One hidden sigmoid layer is introduced (Fig. 1). So the DC current I_d can be easily provided once an MLP network is trained from the DC measurements.

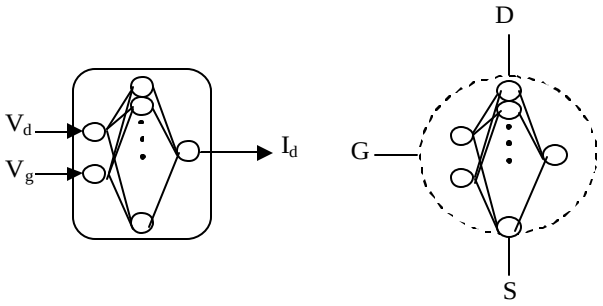

Fig. 1: The neural MOS transistor model and symbol

Small-signal model: The general problem of modeling a MOS transistor in small-signal function can be stated as follows [33]. The nonlinear small-signal drain current I_d^{SS} depends on both the drain-to-source and gate-to-source bias point (V_{d0}, V_{g0}) and the drain-to-source and gate-to-source dynamic voltages over the bias point (v_d,v_g). The instantaneous voltages would be the sum of both voltages, that is, $V_d=V_{d0}+ v_d$ and $V_g=V_{g0}+v_g$. With these premises, our modeling problem consists in finding a function $I_d=f(V_{d0}, V_{g0}, v_d, v_g)$ that provides the estimate of the drain current as a function of the bias and the dynamic voltages.

If the input excitation is small enough, we deal with a so-called small-signal function. In this case, I_d^{SS} can be represented in a small interval around the bias point by the following two dimensional truncated Taylor series expansion:

$$I_d^{SS} = I_{d0} + G_m v_g + G_d v_d + G_m^2 V_g^2 + G_{md} v_d v_g + G_d^2 v_d^2 + G_m^3 v_g^3 + G_{m2d} v_d v_g^2 + G_{md2} v_d^2 v_g + G_{d3} v_d^3 \quad (1)$$

where I_{d0} is the DC current and (G_m, …, G_{d3}) are coefficients related to the nth-order derivatives of the I(V) characteristic with respect to the instantaneous voltages evaluated at the bias point. Therefore, our small-signal modeling problem consists of fitting a function (model) $g : R^2 \to R^{10}$, which approximates the nonlinear mapping from the input space of bias voltages V=(V_{d0}, V_{g0}) to the output space of coefficients of Taylor expansion g(V)=(I_{d0}, G_m, G_d, G_{m2}, G_{md}, G_{d2}, G_{m3}, G_{m2d}, G_{md2}, G_{d3}). Once this model is available, the drain current will be reconstructed by using the truncated Taylor series expansion (6).

So, to be able to model the I_d^{SS} behavior our model must accurately fit not only the nonlinear function but also its n^{th} derivatives. The DC current I_{d0} can be easily obtained from the NN once trained. The Taylor series coefficients should be extracted from DC I_d model by differentiating the NN expression as it is n times derivable. For instance, G_m is given by:

$$G_m = \frac{\partial I_d}{\partial V_g} \quad (2)$$

Consequently, the parameters (G_m, …, G_{d3}) as well as the DC current I_{d0} are the output targets of our unified model. On the other hand, the input patterns are the drain-to-source and gate-to-source, bias voltages.

Once the neural network is trained, it provides, for each input bias point, a set of ten parameters which could be used to reconstruct a small-signal MOSFET model by using the truncated Taylor series expansion. Its block schematic is shown in Fig. 2, the NN to predict the drain current forms the heart of this model.

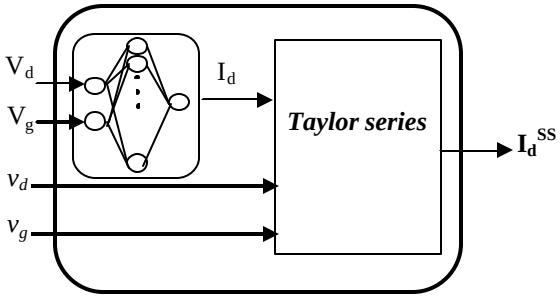

Fig. 2: The block schematic of MOS small-signal model

The modeling process: DC characteristics of transistors can be obtained either from simulations or measurements. The MLP can be trained using such data to produce fast and accurate DC neuromodels. For this work, the training samples are collected by T-SPICE simulations using BSIM3 according to 0.35µm-5V AMS technology. The n transistor length and width are 1µm and 2µm respectively. The device is fully characterized from gathered data with V_g and V_d ranging from 0 to 5V each. DC simulations were taken for the drain current I_d. A training set of 1300 points was used.

The magnitude order of the output parameter I_d is very different, so output scaling is necessary to improve the NN training process. Applying logarithm scale to outputs with large variations balances large and small magnitudes of the output in different regions of the model. Lets $\bar{I}_d = ln(I_d)$ be the scaled drain current that will be the output target of the NN. The inverse transformation is exponential.

Series of neural networks with different numbers of hidden neurons are trained using Levenberg Marquardt algorithm [34]. The MLP with 15 hidden neurons was found to provide the best trade-off between the desired accuracy and the model complexity. A training Mean Squared Error (MSE) of $2.3e^{-4}$ was obtained after 1000 iterations.

The same modeling process is valid to approximate the n and p transistors as having analogous behaviors. A NN with 11 hidden neurons is obtained for a 1µm length and 8µm width p channel transistor.

Model validation: In order to evaluate their generalization capabilities, during the test phase, the neuromodels are used to predict the drain current for gate-source voltage values that are not included in the training set. An example of such result is shown in Fig. 3 where the n model responses are compared with original data. A good agreement of the approximated (neural) and the original (SPICE) characteristics may be noticed.

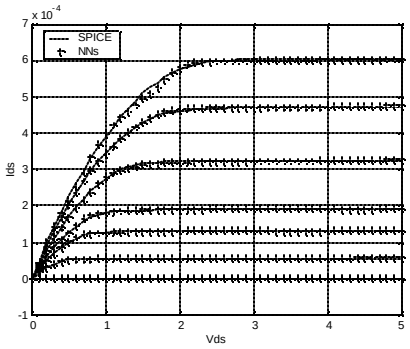

Fig. 3: A comparison of predicted (NN) and original (SPICE) $I_d(V_d)$ characteristics of the n MOS transistor

Fig. 4 shows the Gm parameter curve as an instance of the behavior of the neural model in a small-signal situation.

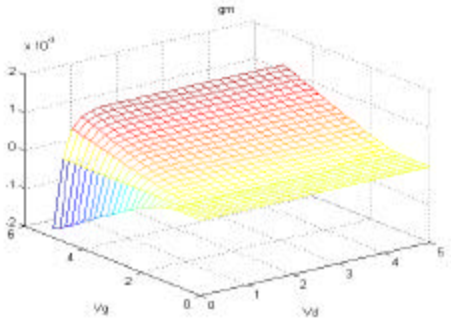

Fig. 4: G_m Parameter provided by the proposed neural model

Implementation into SPICE: As mentioned previously, the main element contributing to the non-linear behavior of the MOS device is the drain current I_d, that is function of the two bias voltages V_d and V_g. So, in SPICE implementation, the MOS may be considered as a voltage-controlled current source. The voltage-controlled current source is a two-terminal DC current supply function of one or more controlling voltages. Its general syntax is given as follows [35]:

gname node1 node2 [cur='expression']

This statement creates a current source according to the expression given between quotes. In our case this expression is determined by the NN function. Indeed, the results of the training process are weights and thresholds associated with the neurons. Besides, a NN is in essence a mathematical equation that evaluates the output variable given input ones. In our case, the NN evaluates the scaled drain current $\bar{I}_d$ in function of the terminal voltages V_d and V_g. Equation 3 corresponds to the expression of the output of the neural model of the MOS type n.

$$\bar{I}_d = \left(\sum_{k=1}^{15} v_k \left(tansig \left(\sum_{i=1}^{2} w_{ki} V_i + q_k \right) \right) + h \right) \qquad (3)$$

where $V_i = \{V_d, V_g\}$, 15 is the number of the hidden neurons and *tansig* is their activation function. w_{ki} and q_k are the neurons weights and thresholds respectively. We used the logarithm scaling to reduce the dynamic of the drain current, so, for the descaling, we apply the exponential function. Therefore, the final expression of the drain current is given by the equation 4.

$$I_d = exp\left(\sum_{k=1}^{15} v_k \left(tan\, sig \left(\sum_{i=1}^{2} w_{ki} V_i + q_k \right) \right) + h \right) \qquad (4)$$

The gate current of the MOS transistor is always neglected and could be modeled by a null current source. So, in SPICE simulations, the implemented MOS model is a subcircuit constituted of a null current source I_g and a voltage-controlled current source I_d which expression is given by the neural function. The equivalent circuit of the MOS is depicted on Fig. 5.

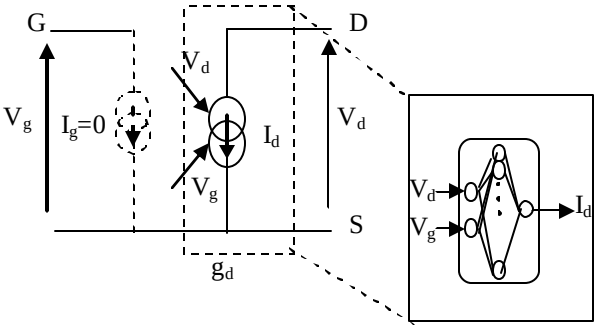

Fig. 5: The new SPICE MOS model

Implementation approach takes advantage of the subcircuit definition option in SPICE. The general form is:

.SUBCKT SubName Node1 Node2 Node3 ...
circuit element lines
.ENDS

A subcircuit definition begins with the .SUBCKT line. SubName is the subcircuit's name. Node1, Node2, etc. are the external nodes. Only these nodes connect outside the subcircuit. The circuit element lines which immediately follow the .SUBCKT line define the subcircuit. The last line in a subcircuit definition is the .ENDS line.

After the implementation of the MOS model into SPICE, it can be used in simulation. This involves two procedures: initializing the model definition within a T-SPICE input file by means of the .subckt statement and instancing the device by means of the instance (x) statement..

The expression of the .subckt of the MOS neural model is given by:

.subckt nmos N_d N_g N_s
I_g N_g N_s 0
g_d N_d N_s

$$\text{cur='} \; exp\left(\sum_{k=1}^{15} v_k \left(tan\,sig\left(\sum_{i=1}^{2} w_{ki} V_i + q_k\right)\right) + h\right),$$

.ends

where N_d is the drain-node, N_s is the source-node and N_g is the gate-node of the device. nmos is the device name.

The device is instanced by:

Xn N_d N_g N_s nmos

RESULTS AND DISCUSSION

In order to demonstrate the merit of our proposal, we simulate with the implemented transistor models some frequently used circuits in DC function, and in small-signal analyses. A comparison with the corresponding SPICE responses will be given.

Neural CMOS inverter simulation: A CMOS inverter is realized by the series connection of a p and n devices [36] as shown in Fig. 6. The nMOS and the pMOS transistors have their gates connected together as the input and their drains connected together as the output.

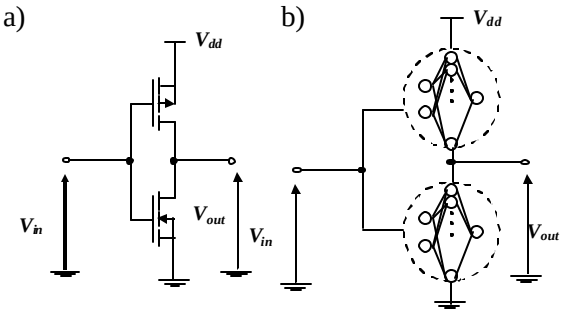

Fig. 6: (a) CMOS inverter, (b) Neural CMOS inverter

The static behavior of the CMOS inverter is simulated using the n and p implemented neural transistor models. Fig. 7 depicts the neural CMOS transfer characteristic. The comparison between the result predicted by the neural CMOS and the SPICE curve (solid lines) can easily be made through the same graphic. Herein, a good agreement may be noticed in the whole domain of interest.

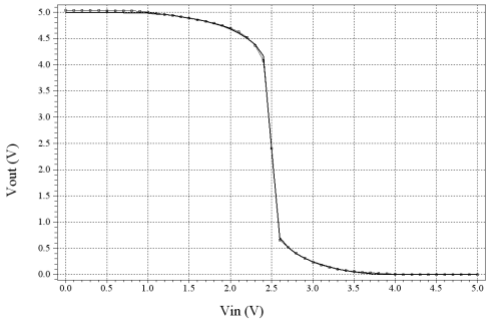

Fig. 7: Comparison of the Neural CMOS transfer characteristic to the SPICE one

MOS Cascode Current Mirror simulation: One of the fundamental analog blocs is the cascode current mirror shown on Fig. 8. Its main function is to duplicate the input current I_{in}. R1 and V_{dc} are not part of the current mirror circuit; they are the load of the circuit. Vdc will be swept from 0 to 5V in order to vary the output voltage from 0 to 5V. Iin will be swept from 0µA to 100µA.

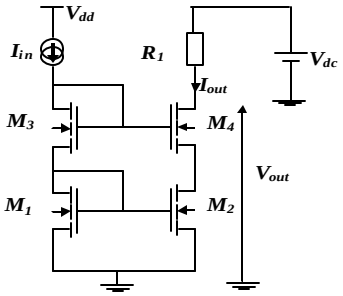

Fig. 8: MOS Cascode current Mirror

SPICE simulation of the cascode current mirror based on the implemented neural models leads to the characteristics depicted in Fig. 9 superposed to the corresponding original curves. The figure shows $I_{out}(V_{out})$ characteristics for different I_{in} values. Good agreement between the original and the neural curves is noticed.

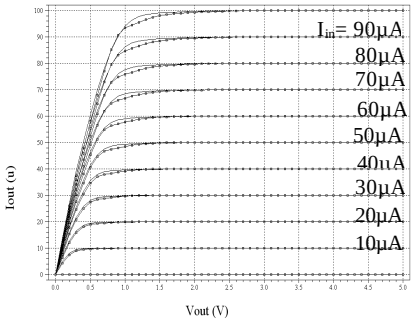

Fig. 9: Simulated performance of the cascode current mirror

Validation on small-signal function: In order to illustrate the small-signal model, an NMOS inverter is used to predict its small-signal current and output voltage and to be compared to the SPICE response. An inverter is constituted of an nMOS transistor in serial with a resistor placed on its drain (Fig. 10). We apply as input a sinusoidal signal of 0.1V amplitude with a DC offset of 1.5V at frequency of 100 Khz.

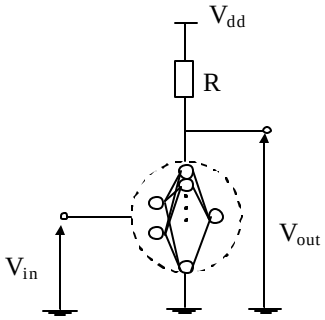

Fig. 10: Neural NMOS inverter

Fig. 11 shows a plot comparing SPICE responses (dashed lines) and the neuromodel results (solid lines) from our approach for the small-signal current and the output of the NMOS inverter.

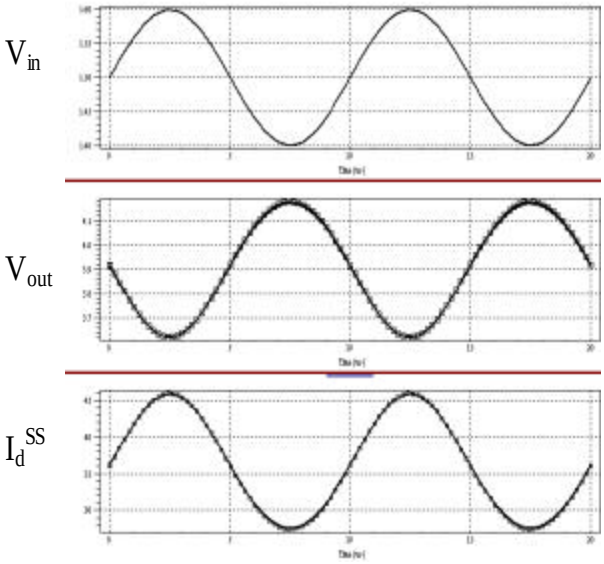

Fig. 11: Response of the neural-based model in small-signal simulation

CONCLUSION

Using the artificial neural networks, we developed a simple, accurate, and fast model for the MOS transistor. The drain current I_d is the main parameter contributing to the non-linear behavior of the device. Being function of the drain-to-source, V_d and gate-to-source, V_g, bias voltages the I_d current was approximated as a voltage-controlled current source and implemented into SPICE simulator. Using the Taylor series expansion, a small-signal model for the MOS device was derived. The extracted small-signal parameters of a device can be used to perform a manual approximated study for any electrical structure.

Comparing simulation results to the SPICE ones, good accuracy and validity were obtained by the proposed approach. The fact, that the outlined approach is versatile and technology independent, makes it a suitable tool for rapid modeling of new devices, and potentially utilized for large-scale circuit simulation. The obtained models may be integrated to SPICE without any additional optimization constraint or compatibility problems. A more generic model for the MOS device is prospected including geometric parameters mainly the transistor length and width dimensions.

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