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Design of Capacitance to Voltage Converter for Capacitive Sensor Transducer

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Abstract: Problem statement: The design of Capacitance to Voltage Converter (CVC) for capacitive sensor transducer was presented. The proposed design will reduce the size, power consumption and supply voltage of the circuit and can be used in high frequency band transducer. **Approach:** The design was implemented using the Operational amplifier (Op amp) and capacitive network. The circuit was simulated using the PSPICE model parameters based on standard 0.13 µm CMOS process. **Results:** The design was able to measure a wide range of capacitance variations for the capacitive transducer. The performance analysis of the design showed desirable performance parameters in terms of response, low power consumption and a linear output voltage within the wide range of capacitive transducer capacitance variation for the power supply voltage of 1.2 V was achieved. **Conclusion/Recommendations:** The output voltage of the circuit varied linearly with the variation of capacitive transducer capacitance variation. The improved converter was compact and robust for integration into capacitive measuring systems and suitable for use in environment that making use of higher frequency band.

Key words: Capacitance, converter, capacitive transducer, sensor transducer, telemetry, measuring systems

INTRODUCTION

Sensor transducers are widely used in the instrument measurement systems such as in the biomedical, automotives, telecommunications, food industry, water treatment plants and chemistry industry. The sensor itself can be defined as a device that can measure (or detect) changes in physical stimulus parameter (such as acoustic pressure, electrical or magnetic field changes, optical, thermal and mechanical) and turns the detected change or measured stimulus parameter signal into a recordable signal or pulse. On the other hand transducers are devices that convert a form of an input energy into a same or another form of output energy. There are many research has been done on the sensor transducers using the capacitance to frequency conversion for the past few years. The sensor transducer is suitably used for converting pressure variations (Takahata and Gianchandani, 2008), humidity measurements (DeHennis and Wise, 2005) into corresponding signal with equivalent frequency. Further, such transducers have been used in water level measurement system or even telemetry systems (Mariun *et al*., 2006; Reverter *et al*., 2007).

Various methods have been reported (Lotters *et al*., 1999; Alia, 2007; Zahirul Alam *et al*., 2009; Ghafar-Zadeh *et al*., 2009; Arfah *et al*., 2010; Chatzandroulis *et al*., 2000) to deal with capacitance to voltage conversion. Some of them, for instance the method utilizing ratio-arm bridge is symmetrical and sensitive, but it has the disadvantage that transformer coils have to be used which is difficult to implement monolithically. Others, for example the modified Martin oscillator with microcontroller is not capable of handling capacitance changes with frequencies higher than 10 Hz. Another approach is based on charge integration (Lotters *et al*., 1999). It is less susceptible to parasitic; however, a fairly large feedback resistor is usually needed to bias the sensing electrode. In the past, the large resistor can be implemented either by sub-threshold transistors or long transistors in triode region (Geen *et al*., 2002). However, values of such MOS (Maiti and Maiti, 2010) resistors depend on the terminal voltages which are difficult to control. For pressure sensor applications, since the capacitance and output voltage of the CVC change over a wide range, the linearity of the feedback resistor degrades seriously. Besides, a large transistor will introduce parasitic capacitance which would cause signal attenuation in a capacitive sensing front-end.

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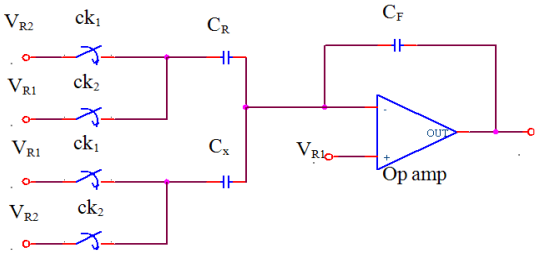

Fig. 1: Capacitance to Voltage Converter (CVC)

In this study the capacitance to voltage converter circuit is designed based on third generation Berkeley Short-channel Insulated Gate FET (IGFET) Model 3 (BSIM3) version 3.2 of 0.13 µm technology and performance of the design is presented.

Proposed ADC architecture: The Capacitance to Voltage Converter (CVC) circuit is designed by using the Operational amplifier (Op amp) by considering the offset voltage of the Op amp and the charge injection error of a switch. The schematic diagram of the CVC circuit is shown in Fig. 1. C_x is the capacitor of the detected sensor and C_R and C_F are the designed capacitors. V_{R1} is the common-mode voltage and V_{R2} is the reference voltage. The signals ck1 and ck_2 are two non overlapping phase clocks. When the signal ck_2 is logic high, the voltage V_{R2} will charge the capacitor C_x, whereas the capacitor C_F stores the offset voltage of the Op amp. When the signal ck_1 is logic high, the capacitor C_F is connected to the output. The voltage V_{R2} charges the capacitor C_R. Thus, by following the principle of charge conservation, the output voltage V_o will be derived as follows:

$$\begin{aligned} &C_x(V_{R2}-V_{R1}-V_{os})+C_R(0-V_{os})+C_F(0-V_{os})= \\ &C_x(0-V_{os})+C_R(V_{R2}-V_{R1}-V_{os})+C_F(V_o-V_{os}) \end{aligned} \quad (1)$$

Therefore:

$$V_o=\frac{C_x-C_R}{C_F}(V_{R2}-V_{R1}) \quad (2)$$

where, V_{os} is the offset voltage of the Op amp and the output voltage is free from Op amp offset as observed in Eq. 2.

MATERIALS AND METHODS

The Op amp plays an important role in designing the converter. Therefore the Op amp is designed based on 0.13 µm CMOS technology.

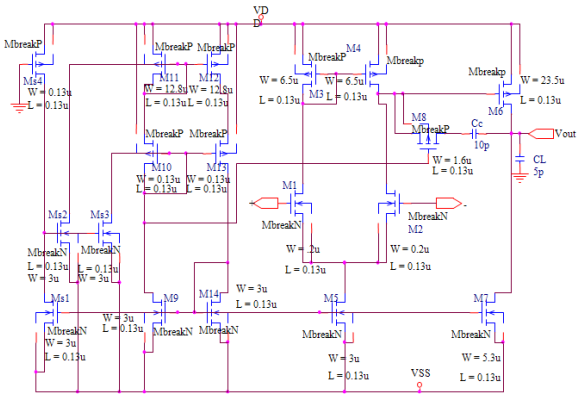

Fig. 2: Schematic for Op amp

The schematic diagram of the Op amp is shown in Fig. 2. The circuit consists of start-up, bias and two-stage Op amp. The Op amp gain is derived as:

$$\begin{aligned} C_x(V_{R2}-V_{R1})=C_x(V_{R1}-OP_-)+C_R(V_{R2}-OP_-)+ \\ C_F(V_o-OP_-) \end{aligned} \quad (3)$$

$$V_{R1}-OP_-=\frac{V_0}{A}, \qquad A: \text{Gain} \quad (4)$$

Therefore:

$$\begin{aligned} V_o&=\frac{C_x-C_R}{C_F}(V_{R2}-V_{R1})\times\left(\frac{1}{1+\frac{1}{A}\left(\frac{C_F+C_R+C_x}{C_F}\right)}\right) \\ &=\frac{C_x-C_R}{C_F}(V_{R2}-V_{R1})\times\left(1-\frac{1}{A\left(\frac{C_F}{C_F+C_R+C}\right)}\right) \end{aligned} \quad (5)$$

It is observed from Eq. 5 that the gain of Op amp should be high so that the output voltage V_O is insensitive of the Op amp gain as mentioned in Eq. 2. The unity gain bandwidth and phase margin of the Op amp need to be considered for stable response and frequency range of operation.

The proposed CVC circuit has been simulated using the model parameters of a standard 0.13 µm CMOS process. The width for the CMOS devices are chosen based on designed equations (Allen and Holberg, 2002; Ali and Khamis, 2005; Nabhan and Abdallah, 2010). The supply voltage of the Op amp is chosen ±1.2V for reducing power consumption.

RESULTS AND DISCUSSION

The voltage transfer a characteristic of the Op amp is shown in Fig. 3. Figure 4 shows the frequency response of the Op amp. The bandwidth gain is approximately 1.8 MHz.

The detection capacitance C_X is varied from 20-1700 fF with the increment of 20 fF. Capacitance C_R and C_F are set to 1 and 1500 fF respectively for this capacitance range. The output voltage waveform with the variation of capacitance, C_X of the circuit is shown in Fig. 5.

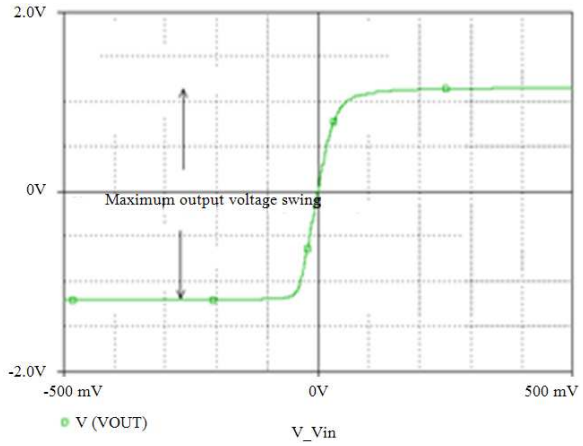

Fig. 3: Voltage transfer characteristics of the Op amp

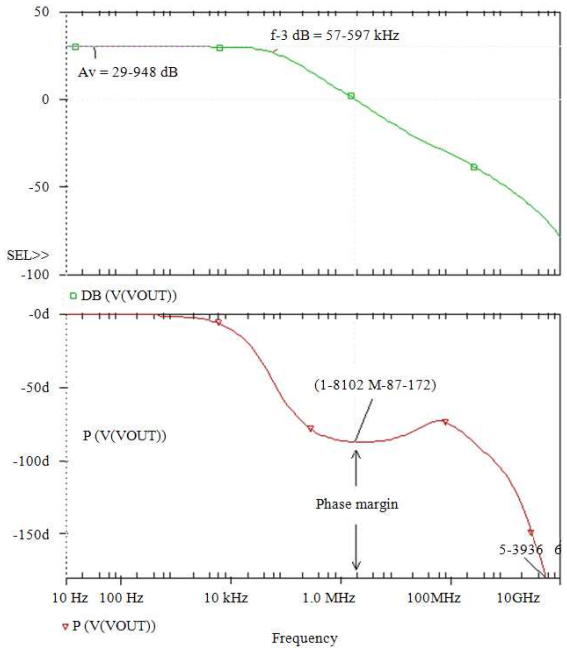

Fig. 4: Gain and phase of the Op amp

The peak output voltage from the Fig. 5 is plotted in Fig. 6 with the variation of C_x. The Fig. 6 shows that the output voltage varies linearly with the variation of C_x.

The operational amplifier differential gain, Ad = 29.948 dB or 31.43 V/V and the 3-dB frequency, f_{-3}dB = 57.597 kHz. Thus, this value of A_d is close to the estimated using the large signal differential transfer characteristic. The phase margin is 92.8° which is more than 60° for stable operation without ringing. The overall performance of the Op amp is tabulated in Table 1.

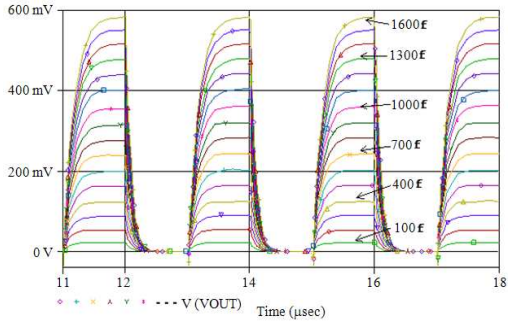

Fig. 5: Output voltage wave form of the converter circuit with the variation of C_x

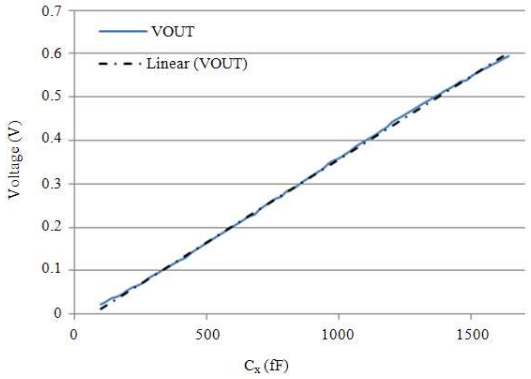

Fig. 6: Peak output voltage with the variation of C_x

Table 1: Performance for Op amp

Specification	Simulation using P spice
Differential gain, A_d	31.43 V/V
Offset voltage, V_{os}	884 µV
Output dc offset, V_{out}	0.0279 V
V_{out} swing range	-1V-470 mV
Open-loop gain, A_V	31.434 V/V
Open-loop gain, A_V	29.948 dB
Unity gain bandwidth, GB	1.8 MHz
Power dissipations, P_{diss}	0.939 mW
Phase margin, PM	92.8°
ICMR	-0.23-1.0 V
3-dB frequency, f_H	57.597 kHz
Slew rate, SR	14 and -19 V µsec^{-1}
Power supply	± 1.2 V

It is noted that the CVC circuit can be used up to 58 kHz.

The value of capacitive transducer, C_x is chosen from 20-1700fF, then any changes of capacitance of the capacitive transducer results linear output voltage within the range of 0.02-0.59V for the variation of the capacitance from 100-1640fF, respectively. The output voltage can be obtained by using following equation:

$$V_o = -0.017 + 3.70 \times 10^{-4} C_X \; 100\text{fF} \le C_X \le 1640\text{fF} \quad (6)$$

where, C_x in fF and V_o in Volts. It is note that the Eq. 6 is valid for the circuit with C_R = 1 fF and C_F = 1500 fF. However, by changing the value of C_R and C_F, other ranges of capacitive transducer can be used. If order to design a circuit that can be detect capacitive transducer capacitance changes within pF range then C_R and C_F are to be chosen in pF range with appropriate ratio.

CONCLUSION

A capacitance measuring systems for sensor transducer was designed in this study is suitable for low voltage applications for less than ±1.2 V. It is observed that the output voltage is linearly varies with the variation of capacitive transducer capacitance within a wide range. Based on these advantages, it is also suitable to be implemented in the pressure, humidity and other sensors applications since it changes over a wide range. The circuit is implementing a short channel technology device that will not only reduce the parasitic capacitance introduced by the transistors but also will benefit to high speed system sensing implementing in lower scale device. The improved converter is compact and robust for integration into capacitive measuring systems and suitable for use in environment that making use of higher frequency band.

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