

## A 2-12 GHz Low Noise Amplifier Design for Ultra Wide Band Applications

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**Abstract: Problem statement:** The Low Noise Amplifier (LNA) is a core block of an Ultra Wide Band (UWB) receiver since it amplifies a very weak signal received at the antenna to acceptable levels while introducing less self-generated noise and distortions. The LNA design poses a unique challenge as it requires simultaneous optimization of various performance parameters like power gain, input matching, noise figure, power consumption and linearity over the entire UWB band. **Approach:** In this study, a three stage LNA is proposed with a resistive current reuse network as a first stage, a cascode amplifier with shunt-series peaking and a local active feedback as a second stage and a voltage buffer as a third stage. A resistive current reuse network is used to achieve better linearity, low noise figure, better input matching with lesser power consumption. A cascode stage with shunt-series peaking and a local active feedback is used to enhance the bandwidth and reverse isolation. A voltage buffer is used as an output stage to achieve better output matching. **Results:** The proposed LNA is designed using 0.18  $\mu\text{m}$  CMOS technology and is simulated to verify its performance. It achieves a power gain of greater than 17.3 dB, a noise figure less than 2.45 dB with an input matching less than -11.2 dB over a 3-dB bandwidth of 2-12 GHz. The achieved output matching is below -12 dB, the reverse isolation is below -68 dB with a Rollet's stability factor is greater than 1000 to ensure better stability. This LNA also ensures better linearity with an  $\text{IIP}_3$  of 3 dBm at 7.5 GHz with low power consumption of 10.7 mW. **Conclusion/Recommendations:** From the simulation results it is evident that the presented LNA claims the advantages of very high gain, better input matching with low noise figure and less power consumption.

**Key words:** Ultra wide band, current reuse, shunt-series peaking, local active feedback, noise figure, input matching

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### INTRODUCTION

In recent years, the academia and industry put forth their interest in UWB technology because this technology offers a promising solution to the Radio Frequency (RF) spectrum drought by allowing new services to coexist with other radio systems with minimal or no interference (Mir-Moghtadaei *et al.*, 2010). UWB technology is suitable for short range and high speed wireless applications which include cognitive radio, ground penetrating radars, imaging and surveillance systems, safety/health monitoring and wireless home video links. In February 2002, the Federal Communication Committee (FCC) approved the First Report and Order (R and O) for commercial use of UWB technology under strict power emission limits for

various devices. The UWB signals must have an average power spectral density not more than -41 dBm/MHz in the 3.1-10.6 GHz band and a bandwidth greater than 500 MHz or fractional bandwidth larger than 20 percent at all times of transmission (Kim *et al.*, 2010; Suresh *et al.*, 2012). Since FCC force stringent power-emission limitations at the transmitter and due to the additional transmission path loss, the received UWB signal exhibits very low Power Spectral Density (PSD) at the receiver antenna. Being the first block in the UWB receiver the main function of the LNA is to amplify this very weak signal received at the antenna to acceptable levels while introducing less self-generated noise and distortions. The design of LNA poses a unique challenge as it requires simultaneous optimization of various performance parameters like

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input matching, noise figure, power consumption and linearity over the entire UWB band with sufficient power gain (Meamar *et al.*, 2010).

## MATERIALS AND METHODS

Most of the recent work done on the LNA have focused on achieving an optimal trade-off between the LNA parameters through different topologies. The distributed amplifier topology provides a moderate gain over a wide bandwidth occupying less area but it consumes very large power (Pino *et al.*, 2010). The CG amplifier topology achieves wideband input matching and better input-output isolation but it exhibits higher noise figure and lower power gain (Chang and Lin, 2011). The inductive source degeneration amplifier provides wider bandwidth, higher power gain and better noise figure. The inductive source degeneration amplifier uses filter networks as matching circuits occupying a very large area (Zhang *et al.*, 2009). The resistive shunt feedback amplifier faces a tough task for providing high gain and low noise figure simultaneously while satisfying impedance matching and flat gain requirements (Yu *et al.*, 2010). The Differential LNA provides high power gain and low noise figure but it suffers from larger power consumption and area (Hwang *et al.*, 2010). The shunt-series feedback amplifier provides a wide band matching and flat gain but it suffers from large power consumption (Hsu *et al.*, 2009).

A current re-used cascade amplifier is proposed in (Yousef *et al.*, 2011) which offer a very high gain over a large bandwidth with a reduced noise figure but it consumes large power and suffers from poor linearity. An improved noise reduction technique comprising of an active positive feedback, input matching extender and transformer is used in (Mehrjoo and Javari, 2011). This topology exhibits very good matching characteristics and consumes low power but its performance is severely degraded at the upper UWB band and it also has poor linearity characteristics. A resistive current reuse technique with dual source degeneration and inductive peaking is proposed in (Wan and Wang, 2011) to obtain noise and input matching simultaneously. This circuit consumes large power and its linearity is very low. A highly linear LNA employing complementary push-pull technique is used in (Galal *et al.*, 2012) but the output matching characteristics are poor and its power performance is also poor.

In this study, in order to reduce the power consumption and to improve the linearity, an UWB CMOS LNA is proposed by the resistive current reuse network as an input stage with a simple filter network

for input matching. The resistive current reuse topology provides low noise figure with low power dissipation and high linearity. The output capacitance of the first stage will limit the bandwidth and it is compensated by an inductor  $L_2$ . A cascode stage with a shunt-series peaking for bandwidth enhancement and a local active feedback for noise reduction and linearity improvement is used as a core amplifier. A voltage buffer is used to obtain an output matching with lesser circuit complexity. The overall gain of the amplifier is calculated after considering the loss introduced by this buffer. The operation of the proposed circuit followed by the simulation results with performance analysis and conclusions are presented in the following sections.

**Proposed low noise amplifier:** The circuit diagram of the proposed LNA is shown in the Fig. 1. The LNA circuit is composed of three stages namely resistive current reuse, cascode with local active feedback and a series-shunt inductive peaking and common drain.

**Input stage:** The small signal equivalent circuit of the input stage is shown in Fig. 2. The gain of the first stage is given Eq. 1:

$$A_{v1} \approx (g_{mn} + g_{mp}) \left( R_F \parallel \frac{1}{s(C_{gdn} + C_{gdp})} \right) \quad (1)$$

The wideband input matching is achieved by the combination the filter network formed by  $L_1$  and  $C_1$ , the input parasitic capacitances of  $M_n$  and  $M_p$  and the feedback resistance  $R_F$  as in Fig. 1. The values of  $L_1$  and  $C_1$  are chosen in such a way that the effects due to Miller capacitances can be adequately compensated at the higher frequencies. The resistor  $R_F$  is used to provide a negative feedback. The gain of the first stage can be increased by increasing the trans-conductance by stacking NMOS and PMOS in complementary push-pull configuration. The input impedance of the circuit is given Eq. 2 and 3:

$$Z_{in} \approx \left( \frac{R_F \parallel \frac{1}{sC_{int}}}{1 + A_{v1}} \right) \parallel \frac{1}{sC_1} \quad (2)$$

Where:

$$C_{int} \approx C_{gs1} + C_{gs2} + (1 + A_{v1})(C_{gdn} + C_{gdp}) \quad (3)$$

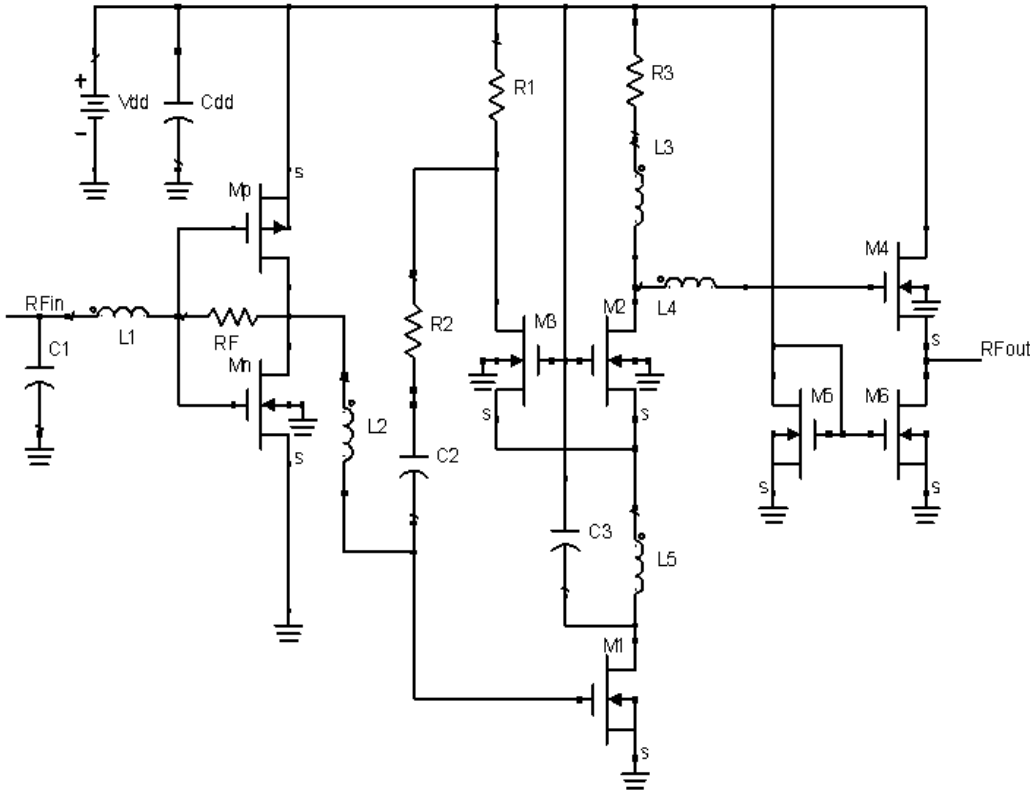


Fig. 1: Schematic of proposed low noise amplifier

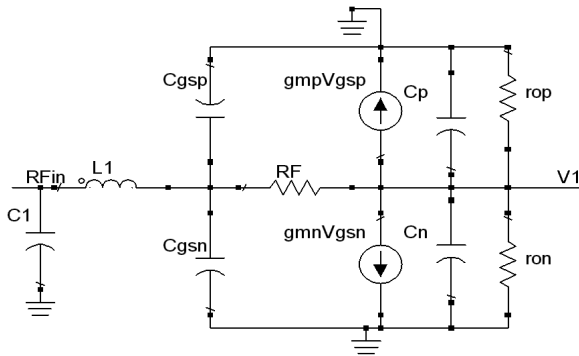


Fig. 2: Equivalent circuit for input stage  $C_p \approx C_{gdp}$  and  $C_n \approx C_{gdn}$

Designing an LNA with high linearity is a challenging task because of the gain reduction and interference due to other standards. In the proposed LNA, the complementary push-pull amplifier is used to improve linearity. The same DC current is used in the two transistors leading to low power consumption. The noise figure of the overall LNA is dominated by the noise figure of the first stage which is the resistive current reuse.

The noise figure of that stage is given as Eq. 4:

$$NF \approx 1 + \frac{R_s}{R_F} \left( 1 + \frac{1}{g_m R_s} \right)^2 + \frac{\omega_0^2 (R_s + \omega_T (C_{gsn} + C_{gsp})^2)}{g_m R_s} + \gamma \quad (4)$$

where,  $R_s$  is the source resistance,  $R_F$  is the feedback resistance,  $g_m$  is the total transconductance,  $\gamma$  is a process dependent parameter,  $\omega_0$  is the resonant frequency of the LC network formed by  $L_1$ ,  $C_1$ ,  $C_{gsn}$  and  $C_{gsp}$  and  $\omega_T$  is the unity current gain frequency which is given as Eq. 5:

$$\omega_T = \frac{g_m}{C_{int}} \quad (5)$$

The 3-dB bandwidth of the first stage is given as in Eq. 6:

$$BW \approx \frac{(1 + A_{V1})}{R_F (C_{int})} \quad (6)$$

From the Eq. 4 and 6, it is evident that the noise figure and bandwidth are traded off. When  $R_F$  is chosen high, the noise figure is low but the bandwidth is also reduced. When  $R_F$  is chosen low the bandwidth is but the noise figure is also high. An optimum value of  $R_F$  is chosen to reduce the noise figure without affecting the bandwidth. In the proposed circuit, the value of  $R_F$  is chosen as  $840 \Omega$  to achieve a low noise figure with acceptable bandwidth. Its value is chosen to be large in order to reduce the noise figure of the input stage and also to achieve a larger bandwidth.

**Cascode stage:** A cascode amplifier with the shunt-series peaking and a local active feedback is used as the core stage. Its equivalent circuit is given in Fig. 3. It compensates for the low 3-dB bandwidth of the previous stage. It further reduces the noise and non linearity at this level with the help of a local active feedback. The cascode configuration provides good reverse isolation as it cancels the effect of Miller capacitance and it also helps in achieving a good gain. The cascode stage also incorporates a current reuse technique that involves the use of cascode transistors along with a drain load inductance  $L_5$  and the loop capacitance  $C_3$ . A portion of the supply voltage is dropped across capacitor  $C_3$  and it is used to bias the upper transistor and therefore it derives less power from the supply. Also at higher frequencies, a low impedance path is created through  $C_3$  as the impedance of  $L_5$  becomes large. So, by using this configuration we obtain flat gain with low power consumption. It is important to understand that a large loop capacitance is preferred in the design for a better signal coupling.

A local active feedback is employed through  $M_3$ ,  $R_2$  and  $C_2$ . The local active feedback can be considered to be made up of two loops viz. the open (gain) loop and the closed (feedback) loop.

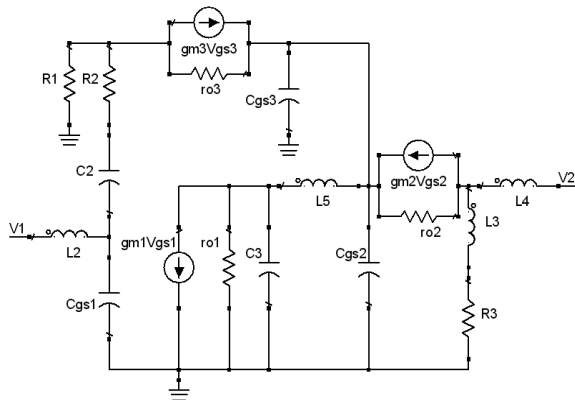


Fig. 3: Equivalent circuit for cascode stage

The open loop is formed by the transistors  $M_1$  and  $M_2$  along with the current reuse branch and it provides very good amplification and output matching. The closed loop comprising of the transistors  $M_1$  and  $M_3$  helps in achieving very good signal coupling between the two stages and a better noise figure with improved linearity. Thus the signal distortion is minimized at the output.

The gain contributed by this cascode stage is given Eq. 7:

$$A_{v2} \approx \frac{A_1 \times A_2}{A_3 \times A_4} \tag{7}$$

Where:

$$A_1 = g_{m1}g_{m2} \left( \left( \frac{1}{sC_3} \right) \parallel \left( sL_5 + \frac{1}{sC_{gs2}} + \frac{L_5g_{m2}}{C_{gs2}} \right) \right)$$

$$A_2 = \left( (sL_3 + R_3) \parallel \left( sL_4 + \frac{1}{s(C_{gs4} + C_{gd4})} \right) \right)$$

$$A_3 = 1 + \beta g_{m1} \left( \left( \frac{1}{sC_3} \right) \parallel \left( sL_5 + \frac{1}{sC_{gs2}} + \frac{L_5g_{m2}}{C_{gs2}} \right) \right)$$

$$A_4 = \left( R_2 + \frac{1}{sC_2} \right)$$

$$\beta \approx g_{m3} \left( \frac{R_2 \parallel \frac{1}{sC_{gd3}}}{R_3 + \frac{1}{sC_3} + \left( R_2 \parallel \frac{1}{sC_{gd3}} \right)} \right)$$

The local active feedback reduces the lower cutoff frequency and increases the upper cutoff frequency thereby enhancing the bandwidth. The series and shunt peaking inductors resonate with the parasitic capacitances, thus the bandwidth is enhanced.

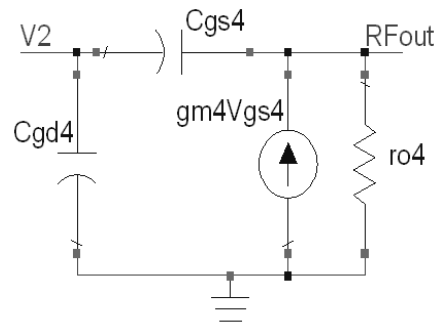


Fig. 4: Equivalent Circuit for Output Stage (without biasing circuit)

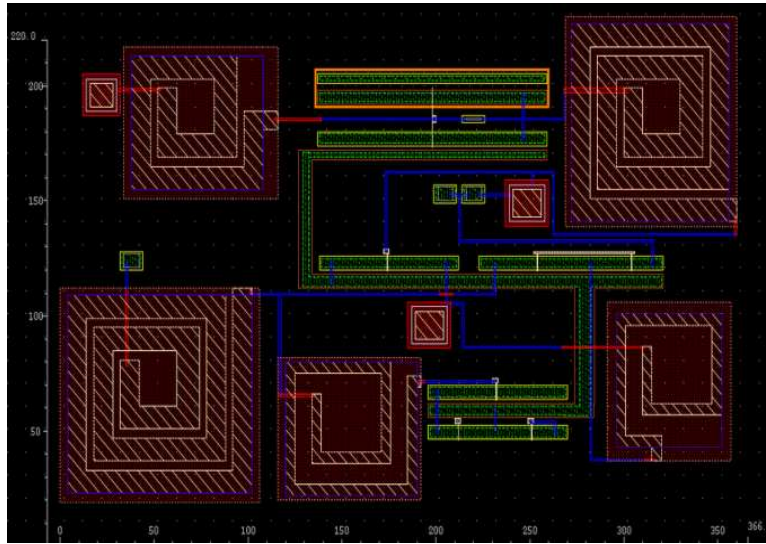


Fig. 5: Layout of the proposed LNA

**Output stage:** The output stage is an output buffer which has low output impedance thereby enabling easy output matching. Its equivalent circuit is given in Fig. 4. The drain resistance of the transistor  $M_4$  serves as the load of the UWB LNA. The load impedance is given Eq. 8:

$$Z_{out} \approx r_{o4} \quad (8)$$

The gain of this stage is given Eq. 9:

$$A_{V3} \approx \frac{g_{m4}r_{o4}}{1 + g_{m4}r_{o4}} \quad (9)$$

The total gain is calculated as Eq.10:

$$A_{VTOTAL} \approx A_{V2} \cdot A_{V2} \cdot A_{V3} \quad (10)$$

The current source used as the load is employed to reduce the nonlinear effects of the buffer.

## RESULTS

The proposed LNA is designed using  $0.18 \mu\text{m}$  CMOS technology and its performance is analyzed by using Cadence RF Specter simulator. The layout of the proposed circuit is drawn using Cadence Virtuoso as shown in Fig. 5. The proposed LNA occupies an area of  $0.1 \text{ mm}^2$ .

The post layout simulation results of the various performance parameters of the LNA are presented on the Fig. 6-12. From the results it has been observed that the LNA can provide an optimal performance in the

UWB band. The proposed LNA exhibits high power gain and linearity thus making it ideal for implementation in UWB receivers.

## DISCUSSION

**Power gain:** The LNA is required to achieve a high power gain in order to reduce the effect of noise introduced by the subsequent stages at the receiver front end. So, in our circuit by using both current reuse and shunt-series peaking techniques, the power gain of higher than 17.3 dB is achieved over the entire bandwidth of 2-12 GHz while the peak power gain of 20.352 dB is achieved at the frequency of 7.5 GHz. This is illustrated in Fig. 6.

**Noise figure:** It is a measure of degradation of the Signal-to-Noise Ratio (SNR), caused by components in the signal chain. The bulk contact of all the transistors in the proposed circuit is grounded in order to reduce the substrate coupling noise. The noise figure of our proposed circuit varies in the range of 2.38-2.45 dB in the entire band as shown in Fig. 7. This ensures that our proposed LNA introduced very little self-generated noise while providing very high gain.

**Input matching:** In general, it is difficult to achieve both noise matching and power matching simultaneously in an LNA design, since the source admittance for minimum noise is usually different from the source admittance for maximum power delivery. In our proposed LNA, a better input matching of less than -11.2 dB is achieved over 2-12GHz with the lowest value being -22 dB at 7.5 GHz by using the simple LC filter along with a local active feedback. This is illustrated in Fig. 8.

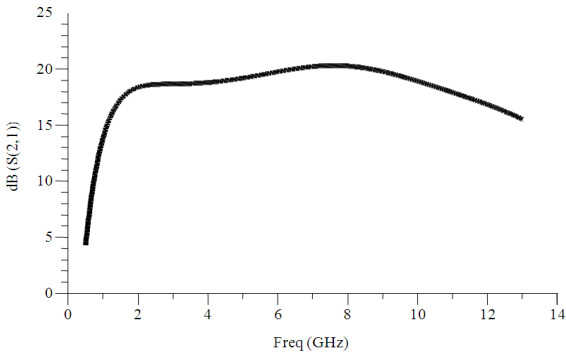


Fig. 6: Power gain ( $S_{21}$ )

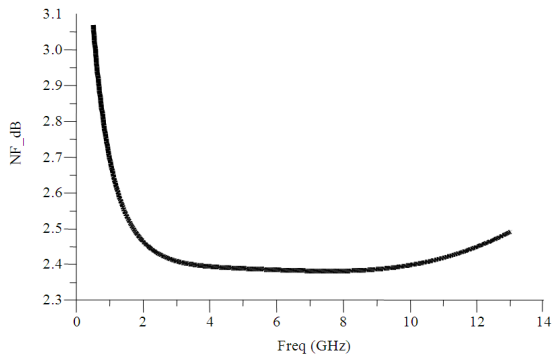


Fig. 7: Noise Figure (NF)

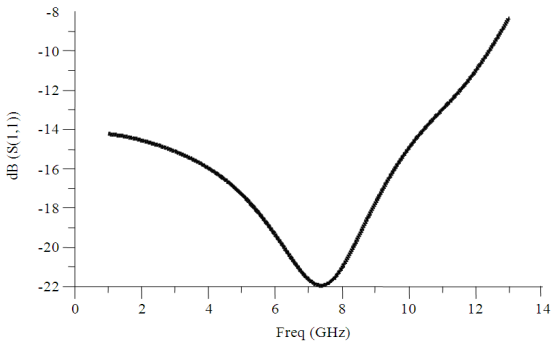


Fig. 8: Input matching ( $S_{11}$ )

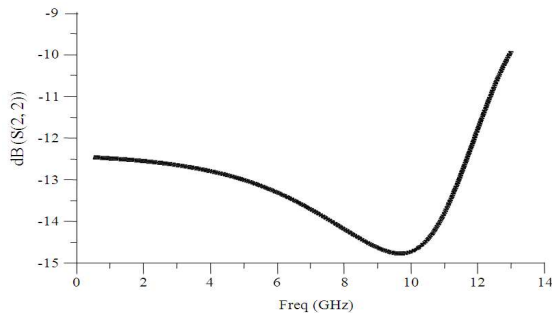


Fig. 9: Output matching ( $S_{22}$ )

**Output matching:** It is also required to make sure the output matching network does not change the DC bias of the active device. Since the source follower is having very low output impedance, it is very easy to achieve the required output matching without any filter network at the output. As shown in Fig. 9, our proposed LNA achieves an output matching of less than  $-12$  dB is throughout the band.

**Reverse isolation:** The input-output isolation ( $S_{12}$ ) is very important parameter to ensure better stability. If the isolation is poor; the output matching will affect the input matching. Since the Cascode stage eliminates the Miller capacitance, it is chosen to provide better isolation. In our proposed circuit a better reverse isolation of less than  $-68$  dB is achieved throughout the bandwidth as shown in Fig. 10.

**Stability factor:** The stability of an amplifier, or its resistance to oscillate, is a very important consideration in a design of an LNA and can be determined from the S parameters, the matching networks and the terminations. The Rollet's stability factor, 'K' is calculated over the frequency band 2-12 GHz by using the Eq. 11. From the simulation results as shown in Fig. 11, it is evident that its value is greater than 1000 and hence the circuit is unconditionally stable (Ullah *et al.*, 2012):

$$K = \frac{1 + |S_{11}S_{22} - S_{12}S_{21}|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{12}S_{21}|} \quad (11)$$

**Linearity:** Linearity is the criterion that defines the upper limit of detectable RF input power and sets the dynamic range of the receiver. The linearity of an amplifier is described in terms of 1dB compression point ( $P_{1dB}$ ) and  $IIP_3$ . This is known as 1 dB compression point and is defined as the level at which the gain drops by 1 dB. For the  $IIP_3$ , the inter modulation products will increase in amplitude by 3 dB when the input signal is raised by 1 dB. Since the UWB signal seldom suffers from gain compression in the LNA due to the low power of the received signal, only  $IIP_3$  is very important. To measure the linearity of the proposed LNA, two test zones of  $-20$  dBm separated by 2 MHz with sweeping frequency range from 2 - 12 GHz is used. From the simulation result as shown in Fig. 12, the achieved in band  $IIP_3$  is 3 dBm in the frequency of 7.5 GHz.

**Power consumption:** As shown in Table 1, the proposed LNA consumes 10.7 mW in 1.2V power supply since it draws a total current of 8.917mA including all the biasing circuits.

Table 1: Power consumption

Freq	I_Probe1.i
0.0000 Hz	8.917 mA

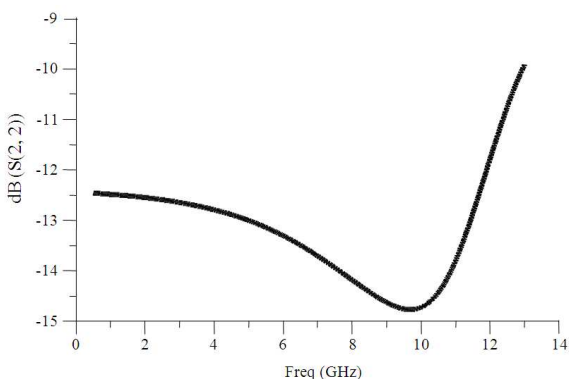


Fig. 9: Output matching ( $S_{22}$ )

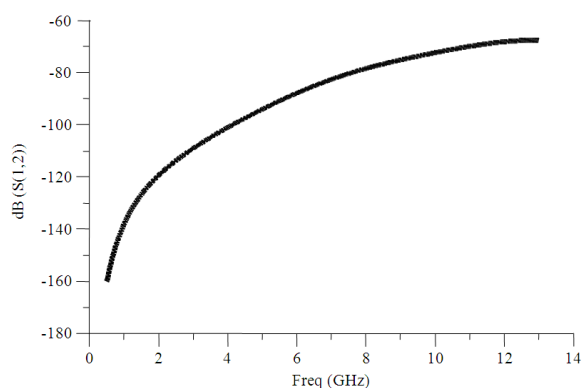


Fig. 10: Reverse isolation ( $S_{12}$ )

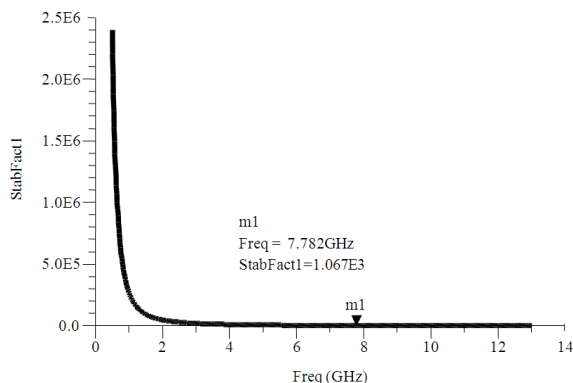


Fig. 11: Stability factor

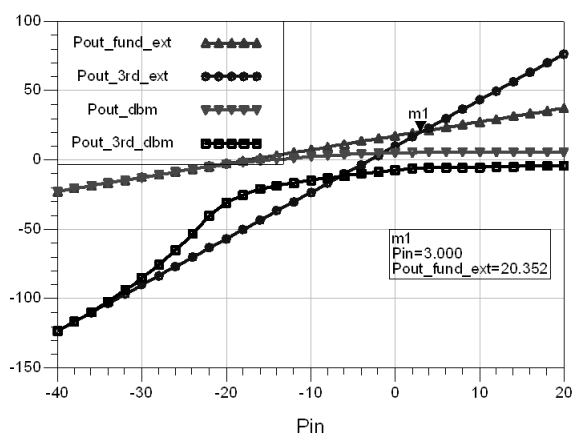


Fig. 12: Third order intercept point ( $IIP_3$ )

Table 2: Simulation results summary and comparison of recently reported CMOS UWB LNAs

References	(Hsu <i>et al.</i> , 2009)	(Yousef <i>et al.</i> , 2011)	(Mehrhojoo and Javari, 2011)	(Wan and Wang, 2011)	This study
Technology	0.18 $\mu\text{m}$	0.18 $\mu\text{m}$	0.18 $\mu\text{m}$	0.18 $\mu\text{m}$	0.18 $\mu\text{m}$
	CMOS	CMOS	CMOS	CMOS	CMOS
BW <sub>-3dB</sub> (GHz)	2-16	2-7.6	3.1-10.6	3.1-10.6	2-12
Gain $S_{21}$ (dB)	10.7-12.3	13.1-13.8	14.8-16	14-16	17.3-20.35
NF (dB)	<2.8	1.85-2.1	2.1- 4.7	2.2-3.4	2.38-2.45
$IIP_3$ (dBm)	-7	-15.2	-7.1	6.4	3
Input Matching $S_{11}$ (dB)	< -8.3	< -10	< -11.5	< -11.2	< -11.2
Output Matching $S_{22}$ (dB)	< -8	-	< -11.2	< -8.8	< -12
Reverse Isolation $S_{12}$ (dB)	-	-	< -45	-	< -68
DC Power (mW)	18.4 @ 1.8V	2.15 @ 1.1V	14.1 @ 1.5 V	16.2 @ 1.8 V	10.7 @ 1.2V

Table 2 presents the simulation results summary our study and comparison of recently reported CMOS UWB LNAs. From the comparison, it is evident that our LNA achieved a very high gain, better input matching with low noise figure and less power consumption.

### CONCLUSION

In this study, the performance of current reuse LNA with local active feedback and a filter network for providing input matching is analyzed. The UWB LNA has been simulated in a 0.18  $\mu\text{m}$  CMOS technology.

The achieved peak power gain achieved is 20.35 dB and the noise figure is less than 2.5 dB in the bandwidth of 2-12 GHz. The input matching achieved is below -11.2 dB and the output matching is kept below -12 dB. The reverse isolation is below -68 dB throughout the entire band. This LNA consumes very low power of 10.7 mW at 1.2 V supply. The presented LNA claims the advantages of very high gain, better input matching with low noise figure and less power consumption.

Since the spiral inductors occupy more area, active inductors can replace them but the circuit should be

designed carefully so that the linearity and noise performance of the LNA is not degraded much.

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