American Journal of Engineering and Applied Sciences

Original Research Paper

A 10GHz Low-Offset Dynamic Comparator for High-Speed and Lower-Power ADCs

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Article history
Received: 20-10-2018
Revised: 17-11-2018
Accepted: 04-05-2019

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Abstract: This paper proposed a design of low-voltage Dynamic Comparator using 90 nm PTM CMOS technology for high-speed and Lower-power Analog to Digital Converter (ADC) applications. The double tail structure is employed as based for design new comparator with positive feedback due to best behavior in low-voltage that allows low delay time; decreases the offset voltage and power dissipation. Simulation results are presented with sampling frequency of $10GH_Z$. These results are also compared with earlier works interms of their delay time, power dissipation and offset voltage. The proposed comparator shows 5.7 mV offset which is small when compared to other dynamic comparators and preamplifier based comparators.

Keywords: Dynamic, 90 nm PTM CMOS, Analog to Digital Converter (ADC), Double Tail Structure Positive Feedback

Introduction

The function of a comparator is to generate an output voltage whose value is high or low depending on the amplitude of the input. Fast and high accuracy comparators can be built using positive feedback circuits periodically enabled and reset by a clock. These synchronous comparators are systematically employed in the implementation of fast Analog to Digital Converters (ADC) and in many other analog systems such as Discriminators, peak detector.

Since comparator is one of the basic building blocks in most Analog to Digital Converters (ADCs). Comparators play a vital role in the overall performance of high-speed ADC converters. As decision-making circuits provide the interface between analog and digital signals, the accuracy, which is often determined by the input-referenced offset voltage, is critical for the resolution of high-performance ADCs. Dynamic comparators are widely used in high-speed ADCs because of its low power consumption and high speed.

In order to show the improvement results of our paper, the new Design based on double tail structure proposed, allows comparing with existing works the fast-speed, low-offset voltage, kickback noise and power dissipation, which are considerably improved. Schematic is drawn using the Ansys Electronics Desktop (Nexxim simulator). This paper is organized as follows. Section II describes the comparator architecture. Section III describes the analysis of the proposed dynamic latched comparator. Section IV provides schematics of various types of dynamic latched comparators. Simulation results using 90 nm PTM technology with V_{DD} = 1V and their comparisons are presented in Section V. Finally, Section VI included Conclusion of the proposed work and future scope.

Comparator Architectures and Previous Works

Designed voltage comparator consists of three stages: Input stage, decision stage and output stage (Mongre and Gurjar, 2014) and the performance of any comparator is defined by the characteristic parameters such as offset voltage (Shaik and Rajesh, 2013), kickback noise (Pedro and Vital, 2006), clock frequency or speed (Iniewski, 2015), low-power consumption (Zbigniew, 2016), high resolution and random noise (Dastagiri and Hari Kishore, 2018). These parameters are mainly considered for design specifications.

Architecture of voltage comparators can be classified in to three types: Open-loop comparators (continuous time comparator), pre-amplifier based latch Comparator (latch with preamplifier) and fully Dynamic Latched Comparator (Shaik and Rajesh, 2013; Iniewski, 2015). However, due to its limited gain-bandwidth product and static power consumption, open-loop comparator are too

slow for many applications. Pre-amplifier based latched comparator employ positive feedback to regenerate quickly voltage difference to full digital levels. It is a combination of Pre-amplifier and latch. Figure 1 shows CMOS differential pair loaded by cross-coupled transistors. The circuits operate between two states: In the reset mode, the switch S_R its closed and positive feedback is disabled (Iniewski, 2015). However, the pre-amplifier based can be reduced latch offset voltage and also the kick-back noise, but suffer to limited gain-bandwidth product static power consumption and reduction of the drain-to-source resistance r_{ds} due to the continuous technology scaling.

The conventional dynamic comparator presented in Fig 2 is preferred to eliminate the static power consumption because this comparator dissipate power only during the regenerative phase and allows a faster operation (Wicht *et al*., 2004; Kale and Gamad, 2010). The operation of the comparator is as follows. During the reset phase when $CLK = 0$ and M_{R3} is off, reset transistors M_{R1} and M_{R2} pull both output nodes V_{out1} and V_{out2} to V_{DD} to define a start condition and to have a valid logical level during reset. In the comparison phase, when $CLK = V_{DD}$, transistors M_{R1} and M_{R2} are off and M_{R3} is on. Output voltages (V_{out1}, V_{out2}), which had been pre-charged to V_{DD}, start to discharge with different discharging rates depending on the corresponding input voltage V_{in1} and V_{in2}. Assuming the case where $V_{in2} > V_{in1}$, V_{out2} discharges faster than V_{out1}, hence when V_{out2} (discharged by transistor M_2 drain current), falls down to V_{DD}-$|V_{thp}|$ before V_{out1} (discharged by transistor M_1 drain current), the corresponding transistor M_{L2} will turn on initiating the latch regeneration caused by back-to-back inverters (M_{L1}, M_{L2} and M_{L3}, M_{L4}). Thus, V_{out1} pulls to V_{DD} and V_{out2} discharges to ground. If $V_{in2} < V_{in1}$, the circuits works vice versa. Nevertheless single-tail Dynamic Comparator shows a high kick-back noise, the small mismatch between differential input CMOS transistor, input-offset voltage in precision applications, such as high-resolution ADC large input-offset voltages cannot be tolerated (Shaik and Rajesh, 2013; Dastagiri and Hari Kishore, 2018).

A conventional double-tail comparator is shown in Fig. 3 (Dastagiri and Hari Kishore, 2018; Rajesh *et al.,* 2016). This circuit enables a large current in the latching stage for fast speed and problems in low power supply voltage, offset input common-mode voltage due to its structure can be overcome, but this comparator requires high accuracy timing between *CLKA* and *CLKB*. Otherwise the desired output may deviate and it results in is increased power dissipation. The operation of this comparator is as follows. During rest phase ($CLK = 0$), M_3 and M_4 are on, charge nodes *Np* and *Nn* to V_{DD} which in turns charges. During evaluation phase ($CLK = V_{DD}$), the tail current transistors *MS*1 and *MS*2 turns on. *Np* and *Nn* nodes common mode voltage decreases and one input dependent differential mode voltage to latch stage. The inverters start to regenerate the voltage difference as soon as the common-mode voltage and the *Np* and *Nn* nodes is no longer as enough for *MC*1 and *MC*2 to clamp the outputs to ground. *MC*1 and *MC*2 also provide additional shielding between the input and output, which in turn reduces kickback noise.

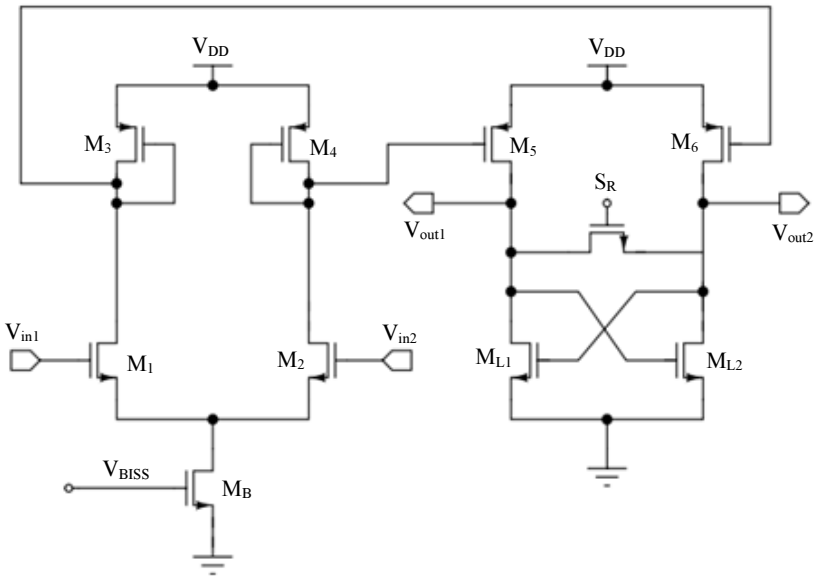


Fig. 1: Pre-amplifier based

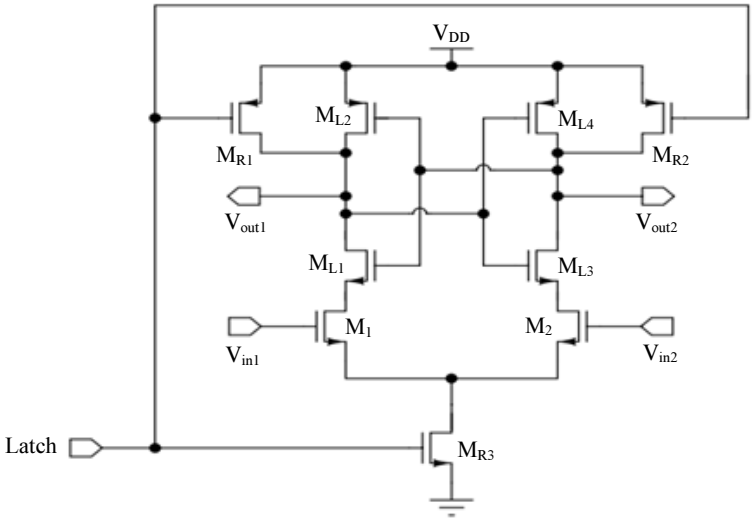


Fig. 2: Conventional dynamic comparator

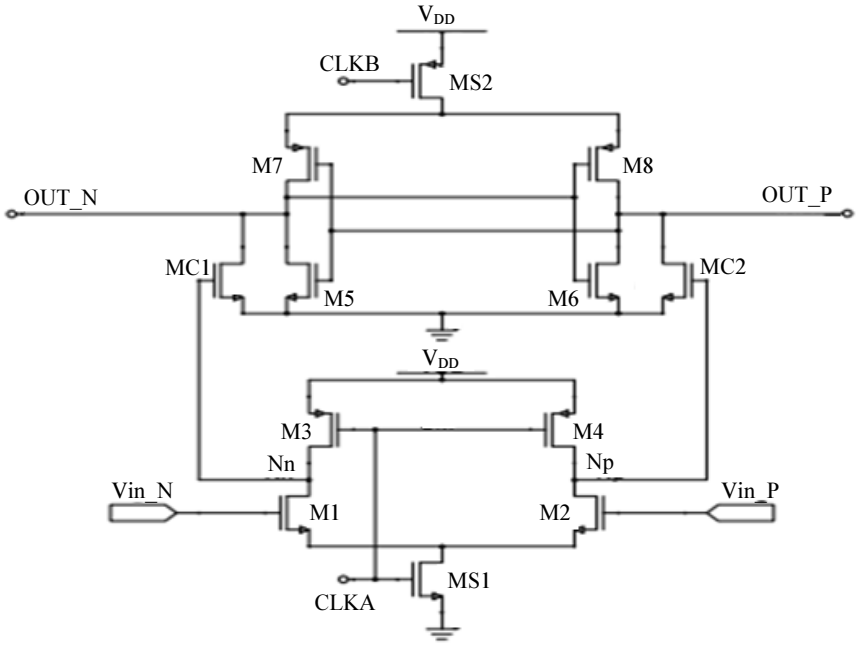


Fig. 3: Conventional double-tail dynamic comparator

Design of the Proposed Dynamic Comparator

The main idea of proposed comparator isto reduce kickback noise by a capacitive coupling between differential input amplifiers. Figure 4 presented the schematic views of the proposed design. The operation is as follows. During the reset phase (*CLK = 0*), both PMOS *M*5 and *M*6 are turned on and they charge *SN* and *SP* nodes capacitance to V_{DD}, which turn both transistor *M*7 and *M*8 to on and *On* and *Op* nodes capacitance discharge to ground while both PMOS transistor *M*11 and *M*12 are being off (no current flows in *M*9 and *M*10 cross-coupled). Comparator *OUT_N* and *OUT_P* are pulled *M*3-*M*4 to V_{DD}, MOSFET *M*13 turn on allow the leakage currents to charge nodes asymmetrically. During the evolution phase (decision-making) when clock signal changes to high state ($CLK = V_{DD}$), *M*5 and *M*6 are now off while *MS* is on and the *SN* and *SP* nodes capacitance discharged from V_{DD} to ground in a different time rate proportional to the magnitude of each input voltage

through transistor cross-coupled and differential input amplifier *M*1-*M*2. When *Vin_N* is large than *Vin_P* (*Vin_N* *Vin_P*), the current in *M3* is larger than the current in *M4*. *SN* node drops faster than *SP* node. The corresponding MOSFETs control: *M*11 turn on, *M7* turn off and *M*4 turn off breaking the connection to the ground (no current flows in the MOSFETS *M*12 and *M*2), then *M*12 turns off. Comparator *OUT_N* node passes to V_{DD}. It forces the other *OUT_P* node to ground and *M*13 turn off. Similarly, when *Vin_N*is less than *Vin_P*, the dynamic comparator works in the opposite direction (or vice versa).

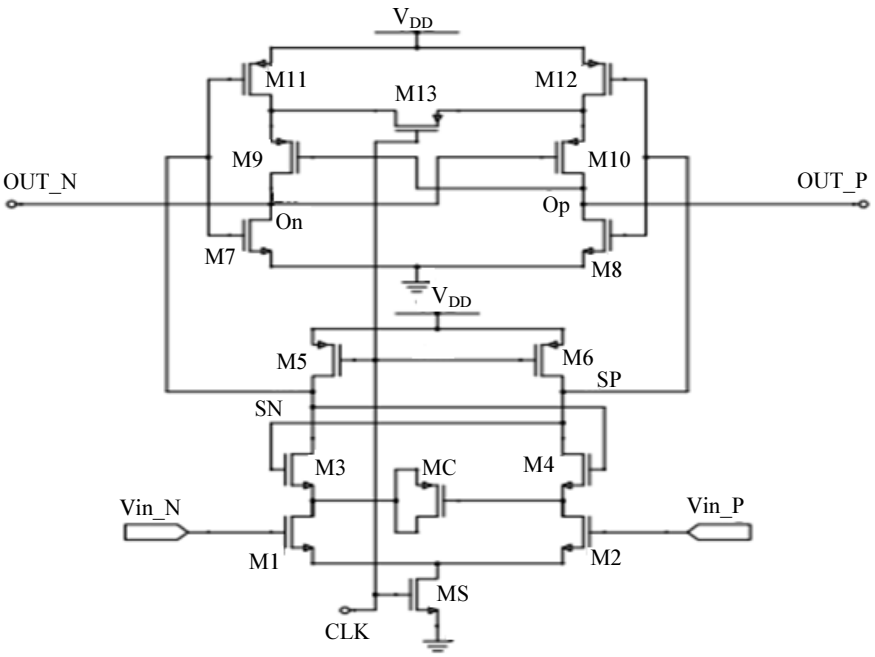


Fig. 4: Proposed dynamic comparator

Schematics of Various Types of Dynamic Latched Comparators

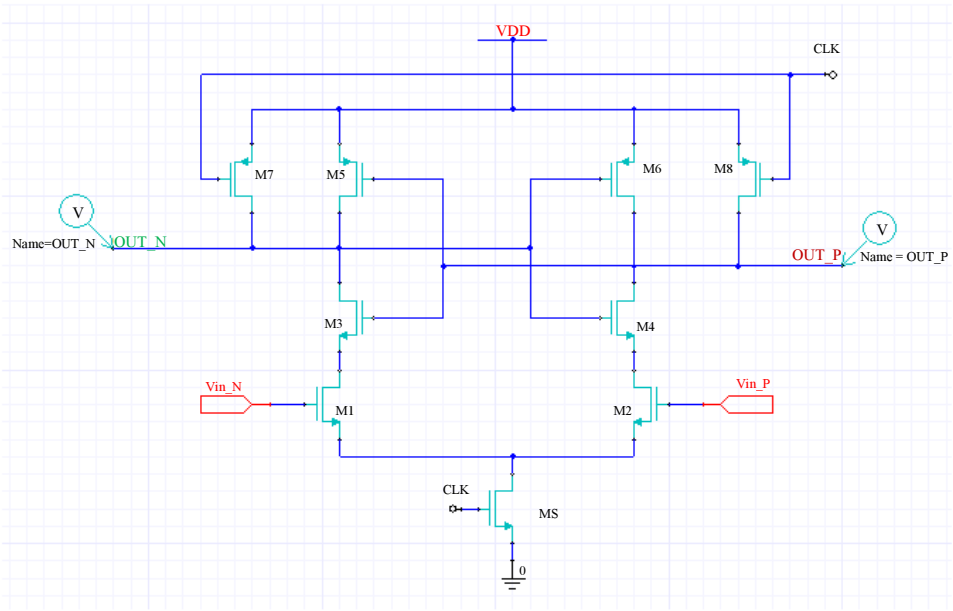


Fig. 5: Conventional dynamic comparator (Comparator 1)

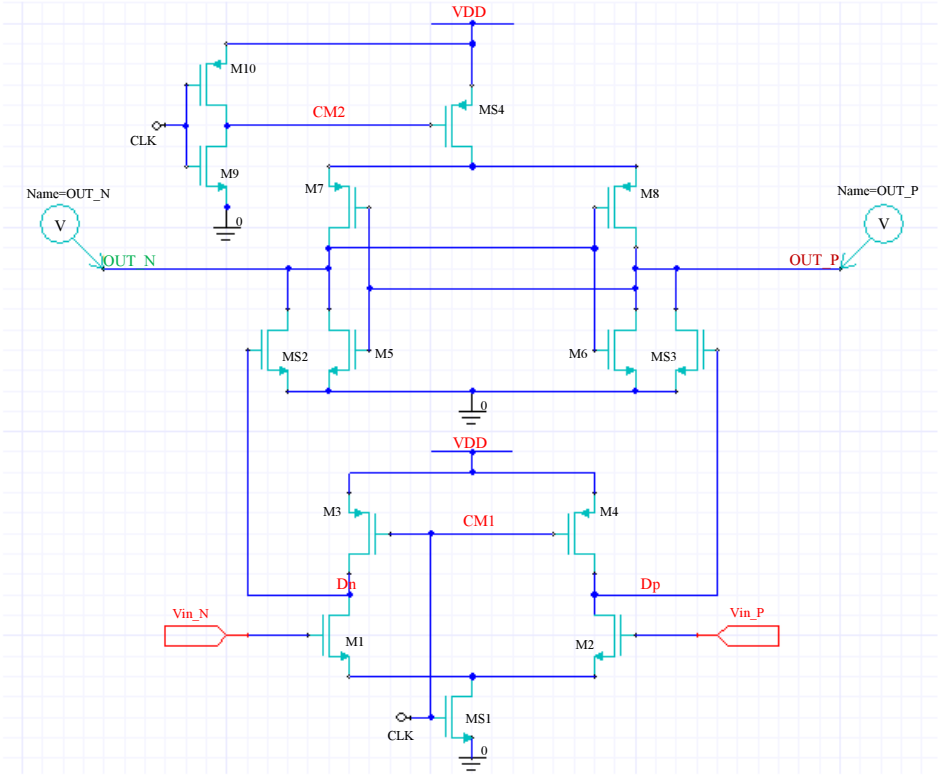


Fig. 6: Double-tail dynamic comparator (Comparator 2)

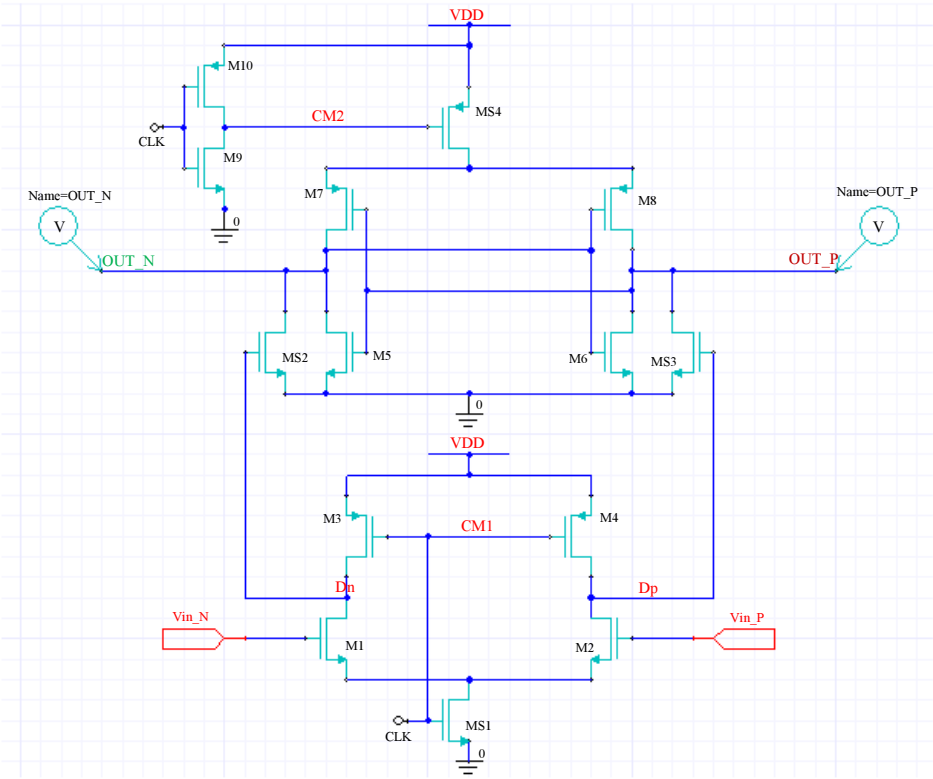


Fig. 7: Dual stage dynamic comparator (Comparator 3)

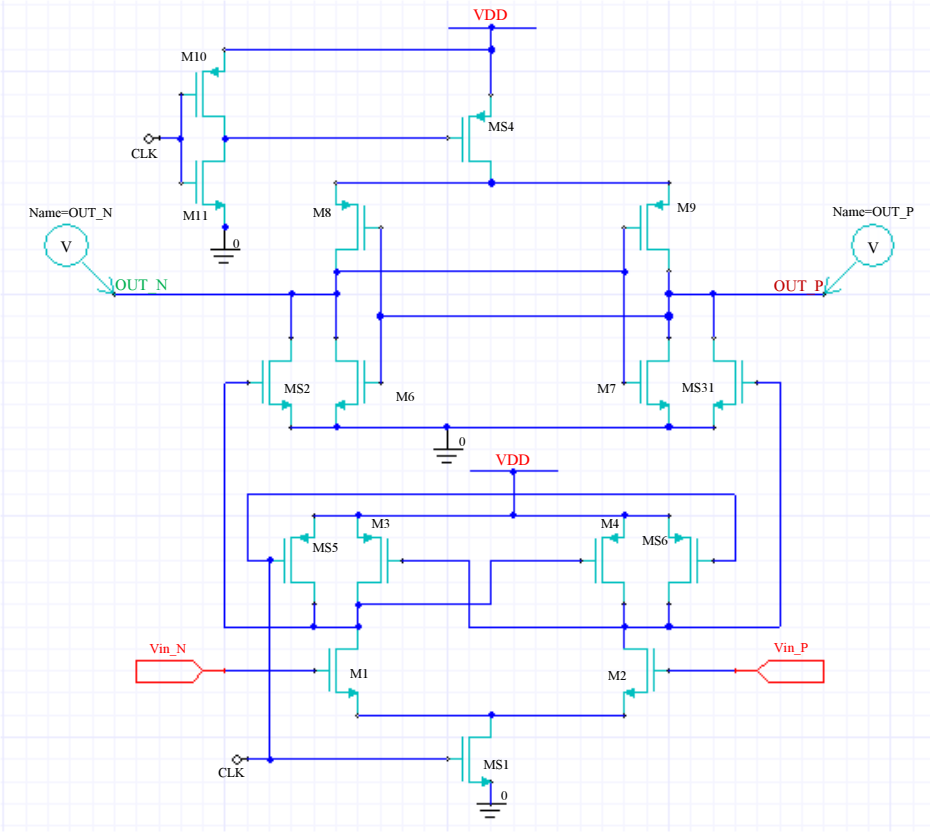


Fig. 8: Proposed dynamic comparator (Comparator 4)

Table 1: Comparison of performance parameters

Comparator type	Number of transistors	Delay (ps)	Power consumption (mW)	Offset (mV)	Kickback noise (mV)
Comparator 1	09	102.00	0.0518	120.0	777.2
Comparator 2	14	70.00	0.1549	20.0	370.0
Comparator 3	16	69.11	0.1528	18.6	310.0
Comparator 4	15	20.23	0.1097	5.7	20.0

Table 2: Comparison of proposed comparator with various supply voltage

	Technology 90 nm	
Supply voltage	Power dissipation	Delay
1.0V	109.7 µW	20.000 ps
1.2V	135.7 µW	18.225 ps
1.4V	165.0 µW	17.090 ps
1.6V	196.7 µW	16.305 ps

Simulation Results and Comparison

In order to compare the performances of the proposed comparator with the previous works, we designed and simulated each circuit using Ansys Electronic desktop with 90nm PTM technology. For simulation of all designs we used, $V_{DD}(max) = 1V$, $f_{CLK}(max) = 10GHz$, $C_{LOAD} = 7fF$, $Temp = 25°C$ and common mode voltage $V_{com}(max) = 0.45V$, $\Delta Vin = 8\ mV$, $fin = 5Ghz$.

Finally, simulations of the comparator designs Fig 5 to 8 are done and simulation results are presented including delay, power dissipation, offset and kickback noise shown in Fig. 9 to 12, respectively. Through simulation, we have obtained parameters of the comparator like power dissipation, offset, kickback noise and time delay. Both existing designs and proposed design is simulated, their results are compared and values are tabulated in Table 1, which show the low power dissipation, low time delay, low offset and low kickback noise parameters as it is required for robustness of the ADCs. Furthermore, when we use the variation of power supply for proposed comparator, the results obtain show the improvement of the time delay and the increasing of power dissipation for the bigger power supply, Table 2.

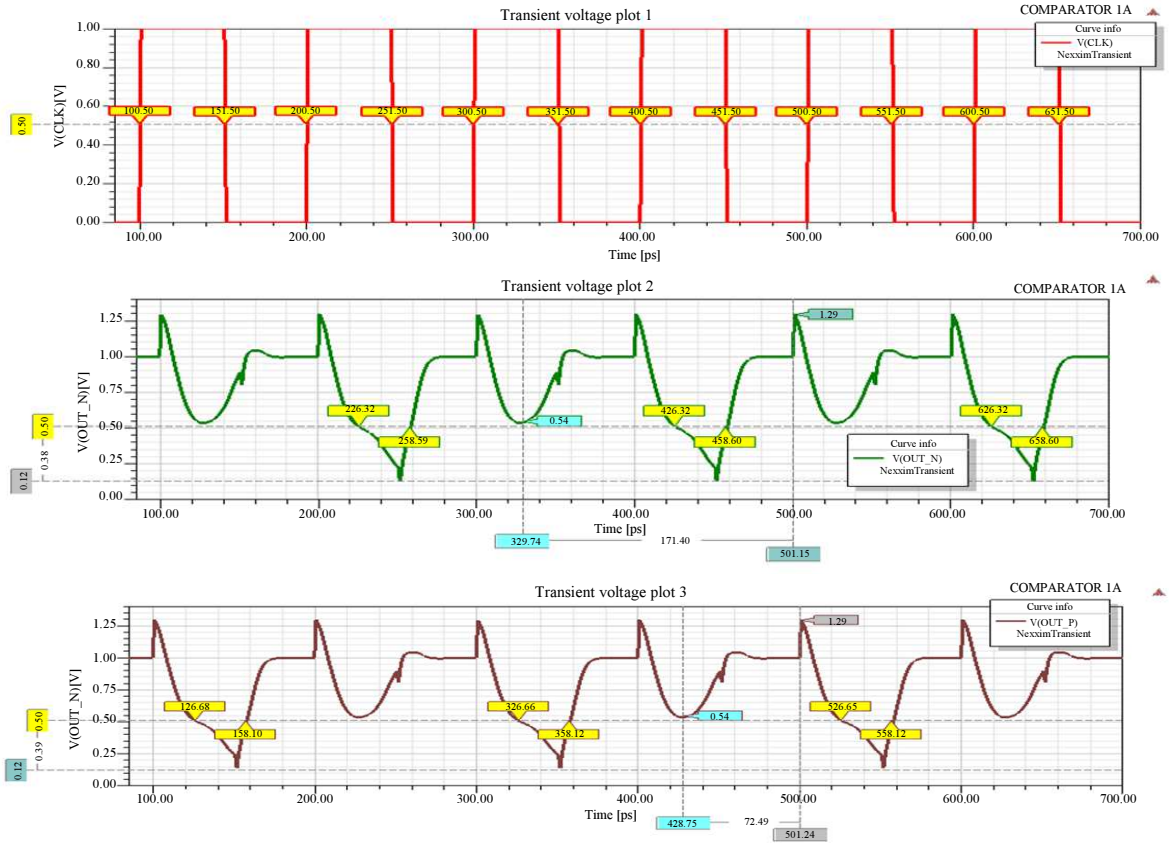
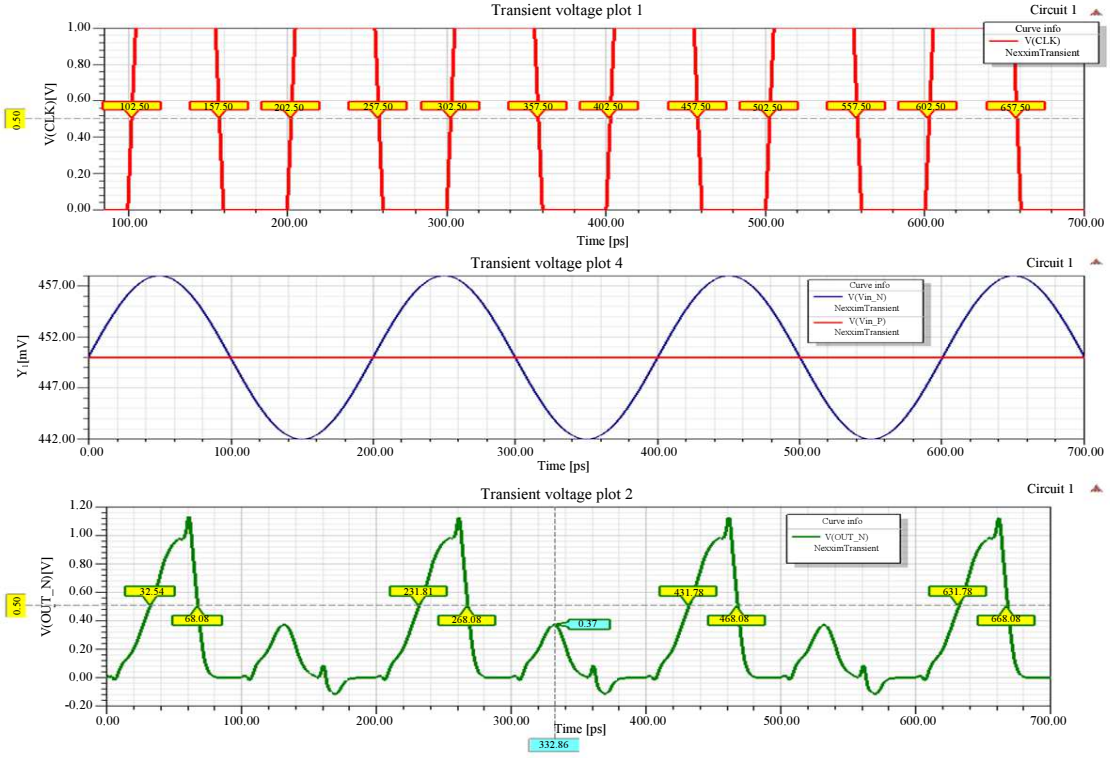


Fig. 9: Simulated waveform of Conventional Dynamic Comparator



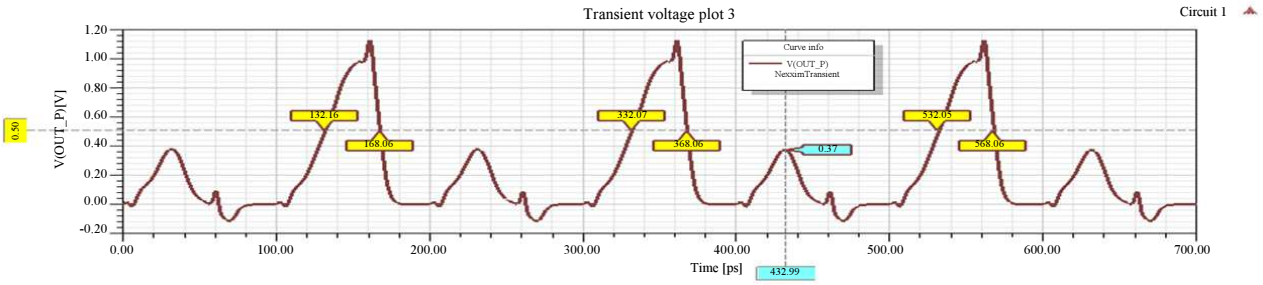


Fig. 10: Simulated waveform of double-tail dynamic comparator

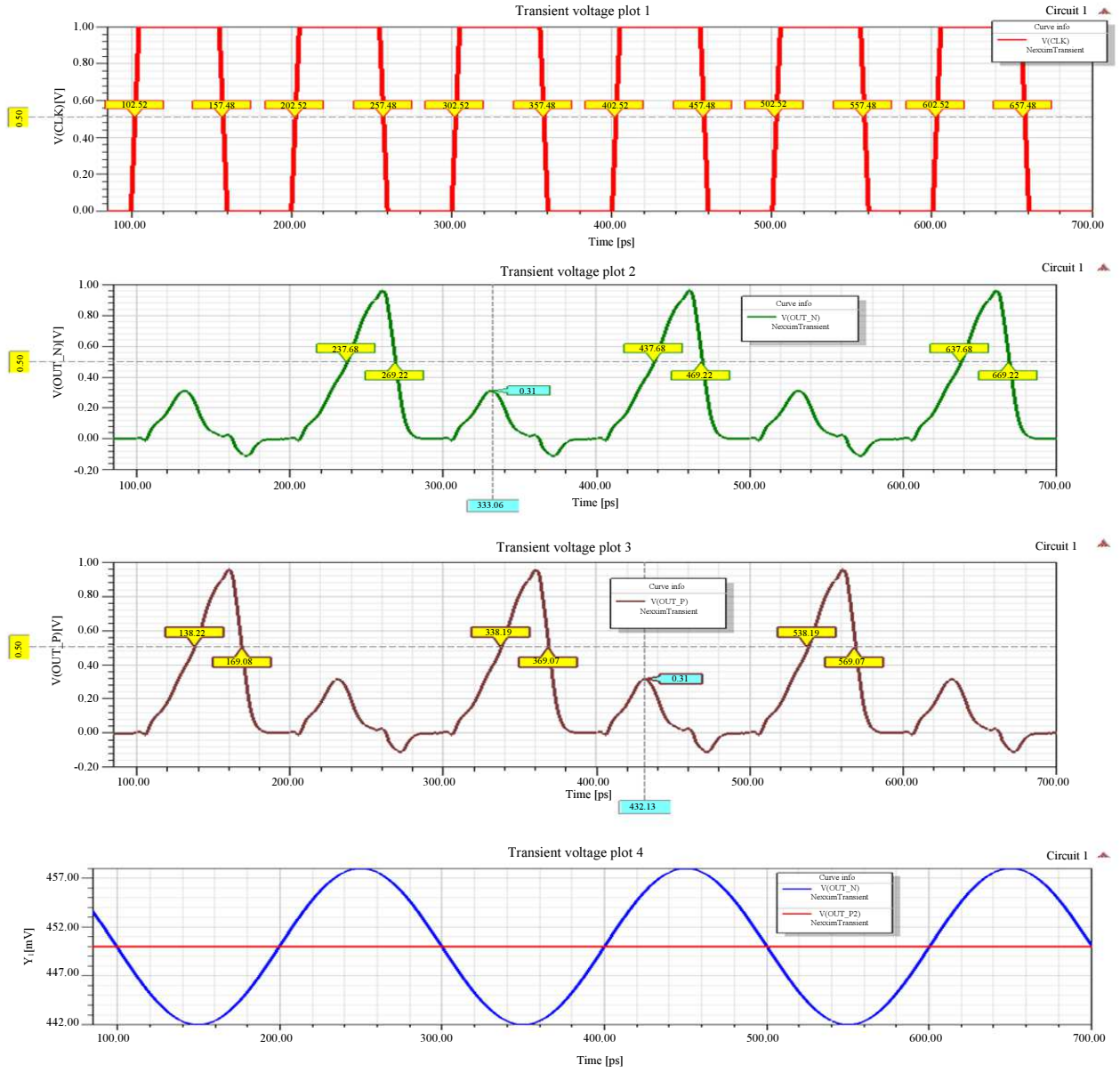


Fig. 11: Simulated waveform of dual stage dynamic comparators

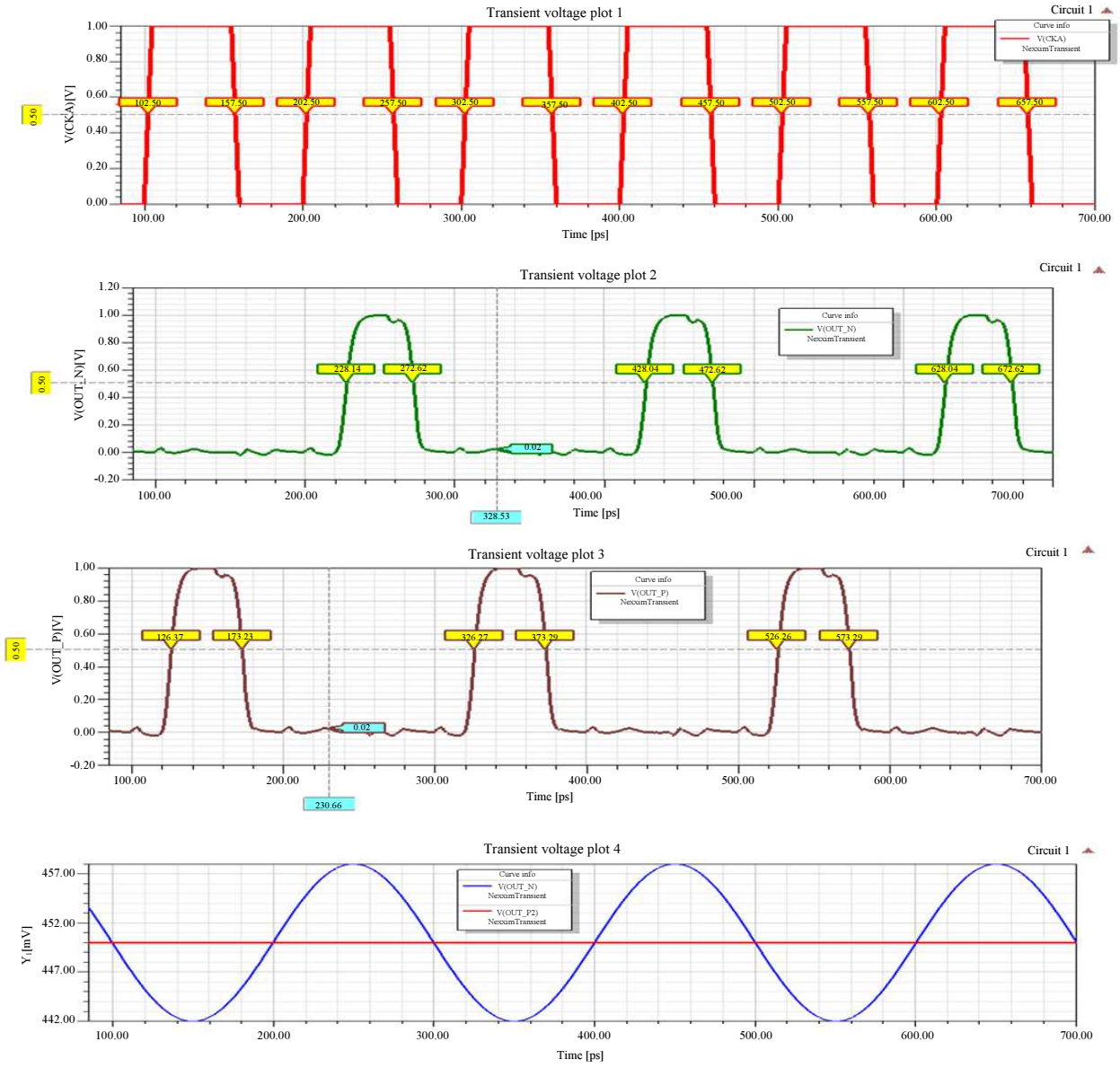


Fig. 12: Simulated waveform of proposed dynamic comparator

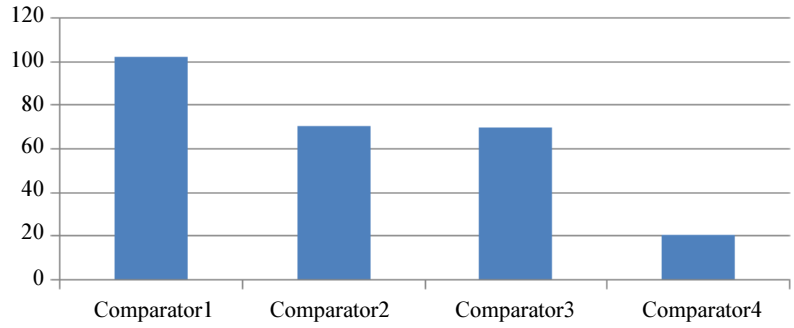


Fig. 13: Delay comparison of dynamic comparators

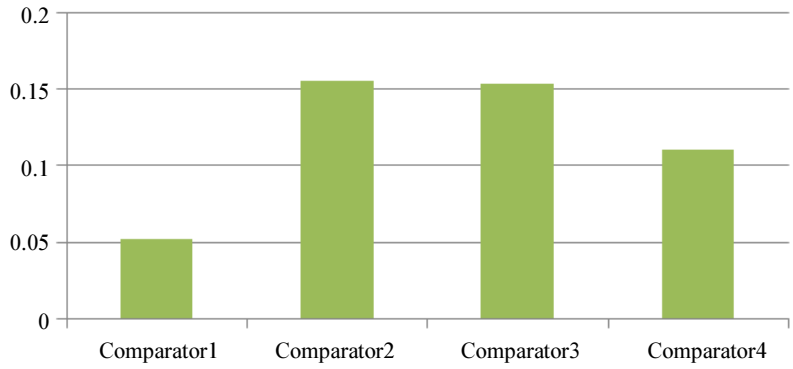


Fig. 14: Power consumption comparison of dynamic comparators

The delay (in ps) comparison of dynamic comparator designs are shown in Fig. 13 in 90 nm technologies.

The power consumption (in mW) comparison of dynamic comparator designs are shown in Fig. 14 in 90 nm technologies.

Conclusion

In this paper, the comparator circuits for high-speed ADCs have been presented. The conventional dynamic, conventional double tail and proposed dynamic comparators have been simulated with 90 nm CMOS technology using Ansys Electronic desktop and their performance parameters such as time delay, power dissipation, offset and kickback noise are compared. The proposed dynamic comparator shows minimal time delay 20.2 3ps, minimal power consumption of 0.1097 mW and 5.7 mV, minimal offset and minimal kickback noise of 20 mVin 90 nm PTM CMOS Technology respectively. The proposed comparator is best suitable for low power and high-speed as it is required for robustness of the ADCs.

Author's contributions

Wembe Tafo Evariste: Project leader, data interpretation and contribute to the writing of the paper.

Bakoune Pierre Hypolite: Design and simulations model. Also, contribute to the writing of the paper.

Moukengue Imano Adolphe: Project leader. Revise and improve the final drafts of the paper.

Ethics

The corresponding author confirms that all of the other authors have read and approved the manuscript and no ethical issues involved.

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