Journal of Computer Science 7 (11): 1629-1632, 2011
ISSN 1549-3636

Braun's Multipliers: Spartan-3AN based Design and Implementation

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Abstract: Problem statement: Multiplication is an essential airthematic operation for common Digital Signal Processing (DSP) applications, such as filtering and Fast Fourier Transform (FFT). To achieve high execution speed, parallel array multipliers are widely used. **Approach:** The field Programmable Gate Arrays (FPGAs) is currently the dominant and viable technology that could be implemented and reconfigured at the same time. **Results:** The Sparatn-3An FPGA resources utilization for 4×4, 6×6, 8×8 and 12×12 bit Braun's multipliers are obtained and Analysis Of Variance (ANOVA) presents that the 12×12 multiplier has significant difference than other three multipliers. The mean delay time for four multipliers shows that as the size of multiplier increases the mean delay time also increases. **Conclusion:** In essence, parallel multipliers based on the FPGA technology can provide better solution for DSP processor, medical imaging and multimedia.

Key words: Application Specific Integrated Circuits (ASICs), braun's multipliers, Field Programmable Gate Array (FPGA), spartan-3AN, Fast Fourier Transform (FFT), Digital Signal Processing (DSP), General Purpose Signal Processing (GPSP)

INTRODUCTION

Real time imaging processes require intensive scientific computations for Digital Signal Processing (DSP). Fast and efficient parallel multipliers are required for DSP, General Purpose Signal Processing (GPSP) and application specific architecture for DSP.

DSP algorithm implementation demands using Application Specific Integrated Circuits (ASICs); costs for ASICs are high as well as algorithms should be verified and optimized before realization. The contemporary Field Programmable Gate Arrays (FPGAs) have emerged as a platform for efficient hardware implementation of such complex and computation intensive algorithms.

There have been reported a number of studys on low power multiplier designs; such as investigation of different multiplier structures (Stouraitis and Paliouras, 2001) introduction of AND gates into multipliers to avoid unwanted spurious transition through the carry save array (Saravanan and Madheswaran, 2008) and switching activity and area of multipliers could be reduced through truncation of the lest significant bits (Rais, 2009a; Rais, 2009b; Rais, 2010a; Rais, 2010b; Rais *et al*., 2010c; Rais and Al Mijalli, 2011a; Rais and Al Mijalli, 2011b).

The objective of this study is to present the 4×4, 6×6, 8×8 and 12×12 bit Braun's multipliers (Yeo and Roy, 2005) and their resources utilization of Spartan-3AN FPGA. Furthermore, ANOVA is applied to see their latency effect in 4×4, 6×6, 8×8 and 12×12 bit Braun's multipliers.

MATERIALS AND METHODS

Architecture platform: For hardware implementation of intensive computations require parallel nature, high frequency and high density of modern platforms. Thus FPGAs are the suitable platforms for such realization of computationally intensive and massively parallel multiplier architecture. Here brief introduction about Spartan-3 FPGA from Xilinx is presented.

Spartan-3 FPGAs: Xilinx family includes Spartan-3 FPGA (Xilinx, 2009) as their fifth generation. Spartan-3 is purposely designed to meet the requirements of high volume, low unit cost electronic systems.

The family comprises of eight member offering densities ranging from 50,000 to five million system gates. The Spartan-3 family includes L, E, A and -3A DSP, Spartan-3AN and the extended Spartan-3A FPGAs.

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Specifically, the Spartan-3AN is used as a target technology in this study. Spartan-3AN combines all the feature of Spartan-3A FPGA family plus leading technology in-system flash memory for configuration and nonvolatile data storage.

The Spartan-3 FPGA consists of five fundamental programmable functional elements: CLBs, IOBs, Block RAMs, 18×18 bit dedicated multipliers and Digital Clock Managers (DCMs).

Braun's multiplier: Braun's multiplier is an n×m bit parallel multiplier and generally known as carry save multiplier and is constructed with m×(n-1) addres and m×n AND gates. The Braun's multiplier has a glitching problem which is due to the ripple carry adder in the last stage of the multiplier.

Basis of braun's multiplier: Consider a generic m by n multiplication of two unsigned n-bit numbers $Y = Y_{m-1} \ldots Y_0$ and $X = X_{n-1} \ldots X_0$

$$Y = \sum_{i=0}^{m-1} Y_i 2^i$$

$$X = \sum_{i=0}^{n-1} X_i 2^i$$

The product $P = P_{2n-1} \ldots P_1 P_0$, which results from multiplying the multiplicand Y by the multiplier X, can be written as follows:

$$P = \sum_{i=0}^{m-1} \sum_{j=0}^{n-1} (Y_i X_j) 2^{i+j}$$

RESULTS

FPGA design and implementation and one way ANOVA statistics: The design of standard 4×4, 6×6, 8×8 and 12×12-bit Braun's multipliers are done using VHDL and implemented in a Xilinx Spartan-3AN XC3S700AN (package: fgg484, speed grade: -5) FPGA using the Xilinx ISE 9.2i design tool. A one-way ANOVA is applied to find out the effect of different multipliers on the mean delay time for Spartan-3AN device.

DISCUSSION

FPGA layouts of the standard 4×4, 6×6, 8×8 and 12×12-bit Braun's multipliers are shown in Figs. 1-4. Table 1 illustrates the statistics of delay in Braun multiplier for Spartan-3AN for 4×4, 6×6, 8×8 and 12×12-bit Braun's multipliers. Fig. 5 shows the mean delay time for the four multipliers, which clearly indicates as the size of multiplier increases the mean delay time also increases, the same result is obtained for truncated multipliers (Al Mijalli, 2011).

Table 2 summarizes the FPGA device resources utilization for standard 4×4, 6×6, 8×8 and 12×12-bit Braun's multipliers.

Table 3 shows the one-way ANOVA on Spartan-3AN FPGA device. The multipliers 4×4, 6×6, 8×8 and 12×12 are used for this analysis. The statistical analysis is done by using Statistical Package for Social Science (SPSS) program. There is a statistically significant difference at the .05 level in delay time for the multipliers ($F(3, 16) = 76.034$, $p = 0.000$). The mean values of delay time for the multipliers are compared by using one-way ANOVA and post-hoc Tukey HSD multiple comparison tests at the .05 significance level.

Table 1: Statistics of mean delay time in Braun's multipliers for Spartan-3AN FPGA

FPGA devices	Bit width	Std. mean (ns)	Std. deviation (ns)	Error of mean (ns)
Spartan-3AN	4×4	12.06	0.7162	0.3203
	6 ×6	13.46	0.5177	0.2315
	8×8	17.22	0.9365	0.4188
	12×12	19.84	1.2837	0.5741

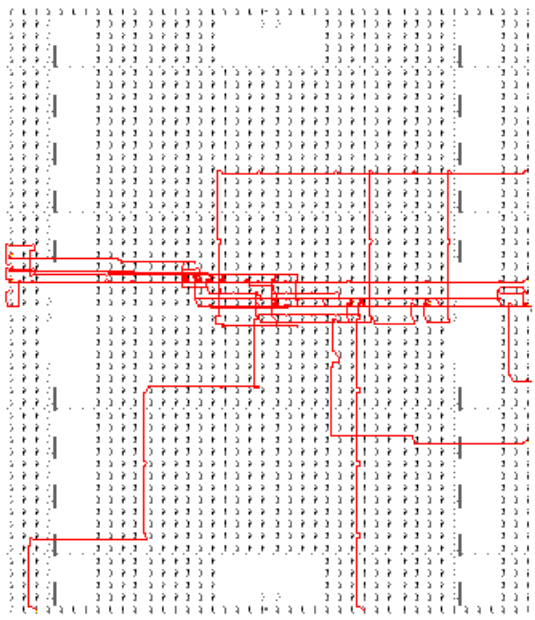

Fig. 1: FPGA layout of 4×4-bit Braun's multiplier

Table 2: FPGA resource utilization for standard Braun's multipliers for Spartan-3AN XC3S700AN (package: fgg484, speed grade:-5)

Bit width	Braun's multiplier	Four input LUTs (11776)	Occupied slices (5888)	Bonded IOBs (372)	Total equivalent gate count	Average connection delay (ns)	Maximum pin delay (ns)
4×4	Standard	32	17	16	192	1.336	3.425
6 ×6	Standard	75	40	24	450	1.007	2.835
8×8	Standard	133	69	32	798	1.325	4.187
12×12	Standard	295	152	48	1770	1.020	4.626

Table 3: Multiple comparisons of delay time (ns) for four Braun's multipliers using Tukey's HSD post-hoc test

					95% Confidence Interval	
(I) Multipliers	(J) Multipliers	Mean difference (I-J)	Std. error	Sig.	Lower bound	Upper bound
4×4	6×6	-1.40000	0.57498	0.110	-3.045	0.245
	8×8	-5.16000*	0.57498	0.000	-6.805	-3.515
	12×12	-7.78000*	0.57498	0.000	-9.425	-6.135
6×6	4×4	1.40000	0.57498	0.110	-0.245	3.045
	8×8	-3.76000*	0.57498	0.000	-5.405	-2.115
	12×12	-6.38000*	0.57498	0.000	-8.025	-4.735
8×8	4×4	5.16000*	0.57498	0.000	3.515	6.805
	6×6	3.76000*	0.57498	0.000	2.115	5.405
	12×12	-2.62000*	0.57498	0.002	-4.265	-0.975
12×12	4×4	7.78000*	0.57498	0.000	6.135	9.425
	6×6	6.38000*	0.57498	0.000	4.735	8.025
	8×8	2.62000*	0.57498	0.002	0.975	4.265

*: The mean difference is significant at the .05 level

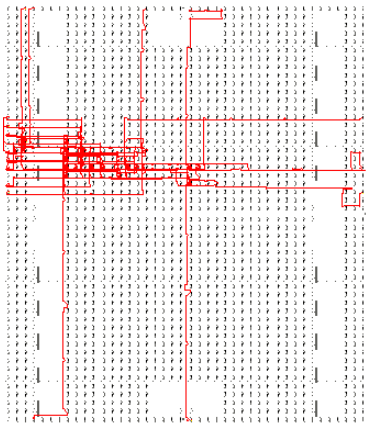

Fig. 2: FPGA layout of 6×6-bit Braun's multiplier

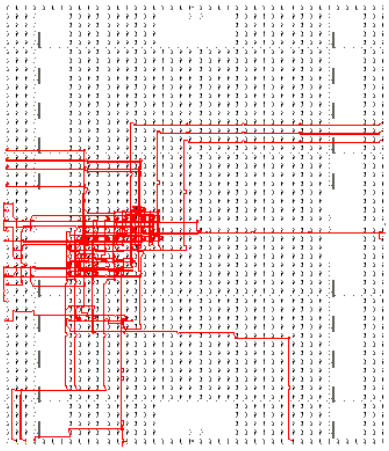

Fig. 3: FPGA layout of 8×8-bit Braun's multiplier

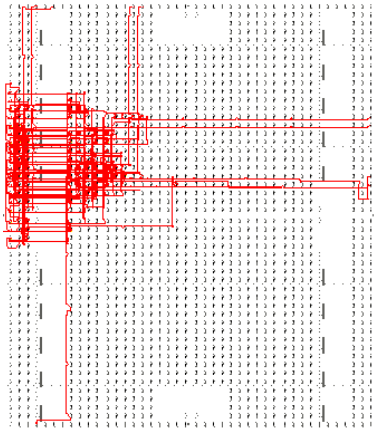

Fig. 4: FPGA layout of 12×12-bit Braun's multiplier

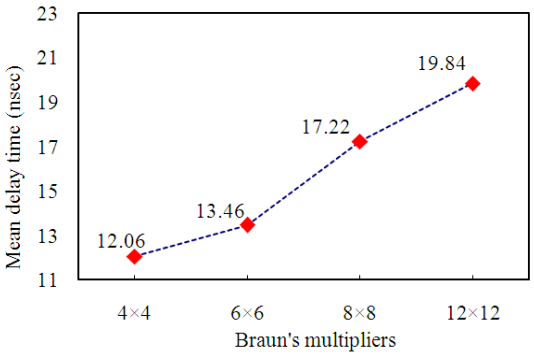

Fig. 5: Mean delay time for the Braun's multipliers

The test indicates that the mean value of the delay time for multiplier 4×4 (Mean = 12.06, Standard Deviation = 0.72) is significantly different from 8×8 multiplier (Mean = 17.22, Standard Deviation = 0.94) and 12×12 multiplier (Mean = 19.84, Standard Deviation = 1.28). There is also significant difference between the delay time for multiplier 12×12 and the others three. However, the delay time for 4×4 multiplier does not differ significantly from 6×6 multiplier.

CONCLUSION

We have presented hardware design and implementation of FPGA based parallel architecture for standard Braun's multipliers utilizing VHDL. The design was implemented on Xilinx Spartan-3AN XC3S700AN FPGA device using the ISE 9.2i design tool. The objective of this study is to present the 4×4, 6×6, 8×8 and 12×12 bit Braun's multipliers and their resources utilization of Spartan-3AN FPGA. Furthermore, ANOVA is applied to see their latency effect in 4×4, 6×6, 8×8 and 12×12 bit Braun's multipliers. The ANOVA presents that the 12×12 and 8×8 multipliers have significant difference than other two multipliers. The delay time for 4×4 multiplier does not differ significantly from 6×6 multiplier. The mean delay time for four multipliers shows that as the size of multiplier increases the mean delay time also increases.

ACKNOWLEDGEMENTS

The researchers acknowledge the assistance and the financial support provided by the Cornea Research Chair, College of Applied Medical Sciences, King Saud University.

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