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Adaptive Complementary Metal-Oxide-Semiconductor Device by Externally Controlled Gate Oxide Thickness

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Abstract: Problem statement: Since the advent of IC and VLSI technology, the demand for high-speed devices and equipment is growing very rapidly. Every individual researcher is marching towards the dream of achieving it. The role of a design engineer is becoming more challenging. As per Moore's law, the packing density doubles every eighteen months. This is possible only by scaling down the device size. This in turn helps in reducing power loss, delay, chip size. In order to achieve high speed switching or frequency the operating voltage as well as threshold voltage must be further reduced which is possible only by downscaling. This scaling down has almost reached its limits, purely because of lack of technology, so further scaling depends on new technology and new material. Rather than waiting for new technology, it would be better to think of changing conventional, single functional NMOS device to a new multifunctional device. **Approach:** In order to understand the concept behind a multifunctional NMOS device, without affecting the device characteristics, it would be good to simulate and analyze the results with known standard results that are available. This approach helps us to understand the device performance and initiates the method or technology to fabricate multifunctional devices. This study deals with the above aspects to understand the new device and its capabilities. **Results:** The characteristic of the multifunctional MOS device is obtained by means of a standard simulation tool. The results show that it allows researchers to think of the new technology for fabrication of such devices. **Conclusion:** If such devices are manufactured at the nano scale, all the above mentioned needs can be met and the researchers can think of new innovative ideas in the area of technology for tomorrow's need.

Key words: Multifunctional device, eighteen months, device performance, micro level, punch through, output current, simulation result, oxide thickness, external current

INTRODUCTION

Nano electronics as a whole is to replace today's devices, in view of future needs. This is because, the next generation expects devices to be operated at speeds of tetra hertz and to be more accurate, while occupying less space. Moore's law states that the packing density of devices in an IC doubles every eighteen months (Chen, 2006). His prediction is proved till today. Researchers are striving to extend his prediction by scaling down the device size. Scaling can be towards the overall device size, but converged towards the gate length. A lot of research stydies have been published in this regard. But scaling is limited due to short channel effect. Channel length cannot be minimized beyond a certain limit. As downscaling exceeds a certain limit, the channel itself vanishes. This is because of the reduction in gate length.

Many methods have been devised and explained to overcome these problems, but the parameters vary as the device size is scaled down (Mead and Conway 1980). Nanotechnology is a new promising area that will really prove its excellence towards making the device multifunctional. This technology will definitely improve the space optimization, low power utilization and most importantly the delay. This study explains the following aspects:

- How the conventional device characteristics at micro level,
- Downscaling and the characteristics of a multifunctional NMOS device
- Methods to realize a multifunctional device
- Special material used to make device multifunctional

All the above aspects are analyzed without compromising the device performance.

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MATERIALS AND METHODS

Device at micro and nano level: At Micro level, designers cannot alter the voltage specification and the material used for fabrication. For any NMOS device, it is by default that the voltage level specifications and the material Characteristics are fixed. The only alternative to improve the performance of the device is by adjusting W (width) or L (Length) or t_{ox} (Oxide thickness). In fact, the most important parameter in the device simulation is ratio of W and L (Pruvost *et al*., 2007, Abdullah *et al*., 2010). The output characteristic of any NMOS device, at micro and nano level is generally split up into two regions, namely linear and saturated region, as shown in Fig. 1 and 2 respectively.

Normalized NMOS device equation at linear region is expressed as given Eq. 1-3.

$$I_{ds} = c_{ox}.\mu.\frac{W}{L}.\left[\left(v_{gs} - v_t\right).v_{ds} - \left(\frac{v_{ds}^2}{2}\right)\right] \quad (1)$$

Here:

$$c_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

Therefore:

$$I_{ds} = \frac{\varepsilon_{ox}}{t_{ox}}.\mu.\frac{W}{L}.\left[\left(v_{gs} - v_t\right).v_{ds} - \left(\frac{v_{ds}^2}{2}\right)\right] \quad (2)$$

Similarly the saturated region is expressed as:

$$I_{ds} = \frac{\varepsilon_{ox}}{t_{ox}}.\mu.\frac{W}{2L}.\left[\left(v_{gs} - v_t\right)^2\right] \quad (3)$$

It is clear that both in linear region and saturated region, I_{ds} is inversely proportional to $t_{ox.}$ Fig. 1 is the simulation result of MATLAB coding (Goldhaber-Gordon *et al*., 1997). The general observations are:

- I_{ds} Can be varied by varying V_{gs}
- Device characteristics are unique and their applications (Selvakumari *et al*., 2009) are limited

The above observations lead to following operational limits:

- Beyond the limits of application of for V_{ds}, a fixed value of V_{gs}, device punch through occurs
- Desired characteristics are achieved at higher voltages
- For every required change in the output current I_{ds}, V_{gs} has to be changed

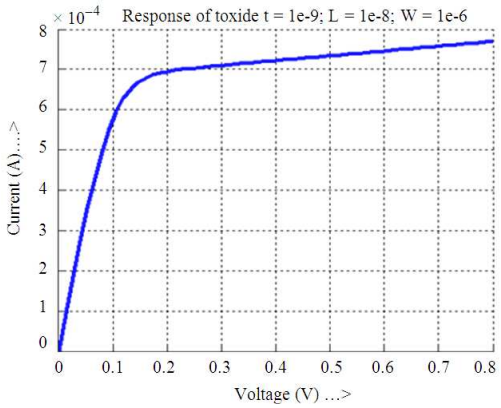

Fig. 1: Simulation result of NMOS device showing output characteristics for oxide thickness t_{ox}=1e-9; W=1e-6

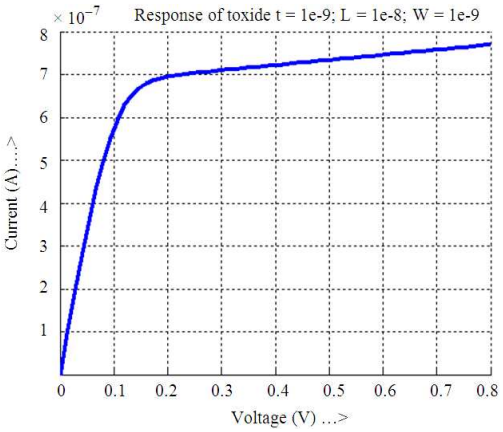

Fig. 2: Simulation result of NMOS device showing output characteristics for oxide thickness t_{ox}=1e-9; W=1e-9

The above limits can be overcome with suitable fabrication techniques. It should be such that:

- Punch through occurs at extended $V_{ds,}$ for fixed V_{gs}
- Desired characteristics are achieved even at lesser voltages, leading to lower power dissipation
- Experiencing the changes in $I_{ds,}$ by fixing the V_{gs} and introducing NEMS concept

It is important to realize that the NMOS device (Chen *et al*., 2011) characteristics at nano level overcome the limits highlighted in the previous section. This is done by a simulation tool. There are some prominent tools available, but here simulation by means of MATLAB is explained. Simulation is done with the objective of overcoming the above limitations, comparing the device performance at micro level and nano level (downscaling).

Table 1: Experimental results of varying the gate oxide thickness from 1e-9-2e-8

		Current (A)			
Voltage (v)	T-oxide (m)	W=1E-6 m	W=1E-7 m	W=1E-8 m	W=1E-9 m
0.2	1 nm	695 µA	69.5 µA	6.95 µA	0.695 µA
0.2	2 nm	418.4 µA	41.8 µA	4.18 µA	0.418 µA
0.2	3 nm	301.4 µA	30.1 µA	3.01 µA	0.301 µA
0.2	4 nm	236.6 µA	23.7 µA	2.37 µA	0.237 µA
0.2	5 nm	195.4 µA	19.5 µA	1.95 µA	0.195 µA
0.2	6 nm	166.7 µA	16.7 µA	1.67 µA	0.167 µA
0.2	7 nm	145.6 µA	14.6 µA	1.46 µA	0.146 µA
0.2	8 nm	129.4 µA	12.9 µA	1.29 µA	0.129 µA
0.2	9 nm	116.6 µA	11.7 µA	1.17 µA	0.117 µA
0.2	10 nm	106.1 µA	10.6 µA	1.06 µA	0.106 µA
0.2	11 nm	97.4 µA	9.74 µA	0.974 µA	0.0974 µA
0.2	12 nm	90.1 µA	9.01 µA	0.901 µA	0.0901 µA
0.2	13 nm	83.9 µA	8.39 µA	0.839 µA	0.0839 µA
0.2	14 nm	78.5 µA	7.85 µA	0.785 µA	0.0785 µA
0.2	15 nm	73.7 µA	7.37 µA	0.737 µA	0.0737 µA
0.2	16 nm	69.6 µA	6.96 µA	0.696 µA	0.0696 µA
0.2	17 nm	65.9 µA	6.59 µA	0.659 µA	0.0659 µA
0.2	18 nm	62.5 µA	6.25 µA	0.625 µA	0.0625 µA
0.2	19 nm	59.5 µA	5.95 µA	0.595 µA	0.0595 µA
0.2	20 nm	56.8 µA	5.68 µA	0.568 µA	0.0568 µA

The simulation result of the device characteristics at the nano level is shown in Fig. 2. It is observed that one of the limitations is overcome, where the output current I_{ds} varies enormously from milliamps to microamps (Table 1). This is achieved by changing the oxide thickness of the device alone and not by changing V_{gs} (Hiroshi et al., 2008). This is an indication of:

- Minimization of power dissipation (pinch off voltage decreasing from 0.6-0.2 v)
- Punch through extension
- Realization of NMOS device at NANO level which is similar to the device at MICRO level in all aspects

The simulation is also tried out for various values of length L, but the results remained unaltered. This clearly indicates that:

- For fixed oxide thickness $t_{ox,}$ current I_{ds} can be varied only by varying V_{gs}
- For the same device, fixing the length L, width W and V_{gs}, I_{ds} can be varied by varying the oxide thickness t_{ox}

Comparing the waveforms of Fig. 1 and 2, it is obvious that the current I_{ds} decrease from milliamps to microamps. Papers were published varying the width, without altering the device performance. The disadvantage is that V_{gs} has to be varied. As an alternative solution, the simulation was done by varying the Gate oxide thickness and fixing the width W, both at micro level and nano level.

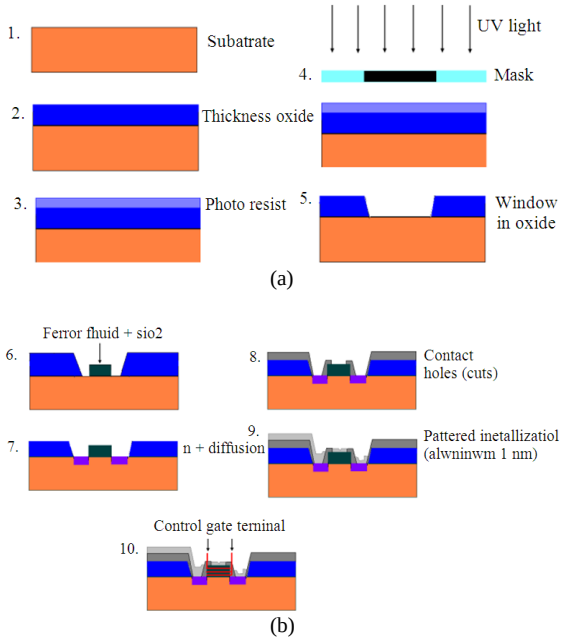

Fig. 3a: Fabrication process of NMOS device, Steps 1-5 (b) Steps 6-9

To achieve the results, a novel material has to be used by replacing the SiO_2 layer which exhibits NEMS concept along with electrical, mechanical and magnetic properties.

The Fabrication process of NMOS device is shown in Fig. 3a and Fig. 3b. The Fabrication Process of NMoFabrication steps for proposed new device: It is now important that the above theory should be realized based on the simulation results. Now the

actual concept of this study is adjusting the Gate oxide thickness. The Hardware implementation by which Gate oxide thickness can be adjusted is explained by means of the fabrication steps:

Steps 1 and 2: Are meant for processing to take place on a p-doped silicon crystal wafer, on which a thick layer of SiO_2 is grown.

Step 3 and 4: Are for masking the substrate with photo resist and exposing it to UV rays respectively.

Step 5: The ultraviolet radiation is exposed to those areas that are to be etched away together with the underlying silicon dioxide, so that the wafer surface is exposed in the window defined by the mask.

Step 6: The important part of this study. In this step the remaining photo resist is removed. Normaly a thin layer of SiO_2 is grown over the chip surface. But here we have proposed a new material.

The new material proposed is Fe_3O_4 mixed with SiO_2, which is used instead of SiO_2. We can now observe the following changes:

- The new material has insulating, elastic, magnetic and electrical property
- This material acts as a substitute for SiO_2
- An additional gate called terminal gate is added along with source, drain and gate terminal in the fabrication itself

The new material Ferro fluid (Fe_3O_4) + Silicon dioxide (SiO_2) is similar to Hydroxyapatite (Wang *et al*., 2009; El-Sayed, 2009).

The material has all the above said properties. When a current is passed through a conductor, magnetic flux is developed externally around the conductor. Now the proposed device must be fabricated such that along with the normal manufacturing process, a few new steps must be added.

The fabrication steps must include an additional terminal apart from source, drain, gate, called as the control terminal. This terminal must be exposed only to the gate region along the periphery. All other regions must be insulated. The new material has the tendency to deform laterally when current is passed through the control terminal. The control terminal is laid along the periphery of the gate terminal. The material being a conductor is partially insulated and partially exposed such that the deformation is along both positive and negative y-axis direction. The magnitude of deformation depends on the amount of external current applied. This deformation varies the Gate oxide thickness t_{ox} which in turn varies the output current I_{ds}. Normally I_{ds} varies when V_{gs} is varied. But here output current I_{ds} varies with respect to external current and not by varying of V_{gs}. This concept is very unique to the proposed new device and can be realized only with the new material.

The remaining Steps 7-9 diffuses n + region into areas where thin oxide is removed. Transistor drain and source are self-aligning with respect to the gate structures. Then Grow thick oxide overall and then etch for contact cuts. Finally deposit metal and pattern with overglassing.

Proposed (ESWV) Algorithm (externally stressed gate oxide thickness Variation): The logic behind varying the Gate Oxide thickness is now discussed. The algorithm is designed to see that the device performance is maintained for various values of Gate oxide thickness. The algorithm is:

Step 1: Initialize all parameters. (Width, Gate oxide thickness)

Step 2: Calculate the gate capacitances (source, Drain, Gate capacitances)

Step 3: Initialize the Gate oxide thickness to micro Units and control current to Zero.

Step 4: Plot the graph of output characteristics for output current and Gate oxide thickness.

Step 5: Change the Control gate current to new value.

Step 6: Repeat Steps 4, 5 for various values of the Control gate current.

RESULTS

Simulation Results and Analysis of varying Gate oxide thickness: The oxide thickness of the gate material is assumed such that, under external application of stress, it deforms in its area. This results in variation of material resistance and thereby the drain current $I_{ds.}$ This function is useful for the device that is proposed in this study (Chen *et al*., 1996). Fig. 4 relates the Gate oxide thickness variation and corresponding drain current (Kawata *et al*., 2007, Grabert, 1991). The simulation result reveals that:

- The device can be operated at high currents (range microamps to milliamps)
- The same device can be used as multifunctional device and can be operated at low voltages thereby leading to lower power dissipation
- Punch through can be extended

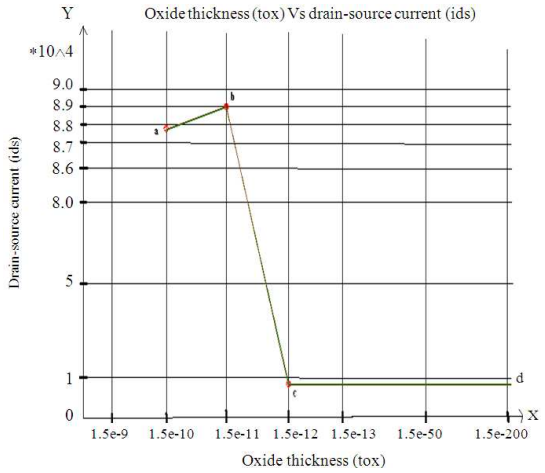

Fig. 4: Simulation result of NMOS device showing output characteristics for oxide thickness vs. Drain source current

Graph a b = Current variation is predictable:
Graph b c d = Current variation is unpredictable: From Fig. 4 the current variation (Graph a b) is predictable and (Graph b c d) is unpredictable. So we take the region (Graph a b) for complete analysis.

Fig. 5 is the simulation result of MATLAB coding. The general observations are:

- I_{ds} can be varied by varying the t_{ox} level of 1e-9-20 e-9.
- Same device can be used as a multifunctional device and can be operated at low voltages, thereby leading to lower power dissipation .
- Punch through can be extended.

DISCUSSION

The graphical result clearly indicates that adjusting the Gate oxide thickness will change the device characteristics. The adjustment is very small but it is tried out merely to verify the logic. Though the simulation result seems valid, the variation in Gate oxide thickness should be considered. It suggests a way to proceed further and to have the device function as a multifunctional device. The drain current varies from milliamp to microamp as the Gate oxide thickness increases. All these changes happen for fixed gate voltage.

Normally this happens for varying gate voltages. It is this aspect which makes the device multifunctional. Hardware design engineers may need to keep this point in mind have the device Gate oxide thickness to be adjustable so that the device is multifunctional. This is where NEMS can play a vital role (Goser *et al*., 2004; Likharev, 2008).The simulation can be further fine-tuned to realize the practicality.

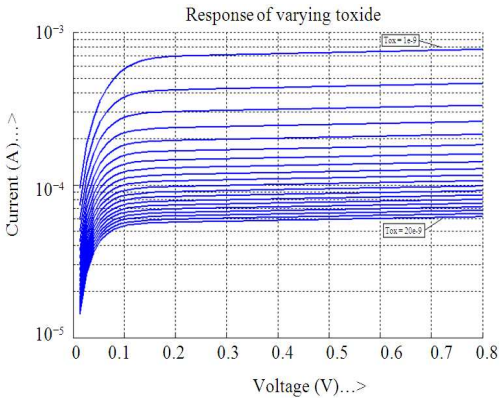

Fig. 5: Simulation result of NMOS device showing output characteristics for oxide thickness variation at nano level

The objective of this study is to see that the device size is reduced and also made multifunctional. So simulation is tried by increasing the value of the Gate oxide thickness from 1e-9-20e-9. The results are shown in Fig. 5 and the corresponding experimental Values of Drain currents are shown in (Table 1). Here the simulation result seems practically possible but the actual concept is that, rather than to depend only on electronics to fabricate a new device, other engineering disciplines can also be considered, particularly, mechanical, magnetic aspects, that can make the new device heterogeneous (Iwai *et al*., 2004, Cuniberti *et al*., 2010). Here selection of new material plays a vital role.

Fig. 5 clearly indicates the response of the proposed device if fabricated. It is merely using the hybrid technology that combines the properties of electricity, magnetism and elastic property. A new material which is combination of Fe_3So_4 and SiO_2 is to be experimented to achieve the required characteristics. Even other materials especially nano composites, colloids may also be tested for manufacturing this type of device.

The selected material must possess electric, magnetic and elastic properties. When such materials are used they should not alter the device performance. If such a device is fabricated, then we can realize a device which is multifunctional.

It is clear from Table 1 that the current decreases constantly at the rate of 1/10th of the previous value. This is the advantage of the new device proposed (Haron *et al*., 2009).

This ensures that power consumption is minimized. The role of a design engineer in fabricating such a device should be to satisfy the following points:

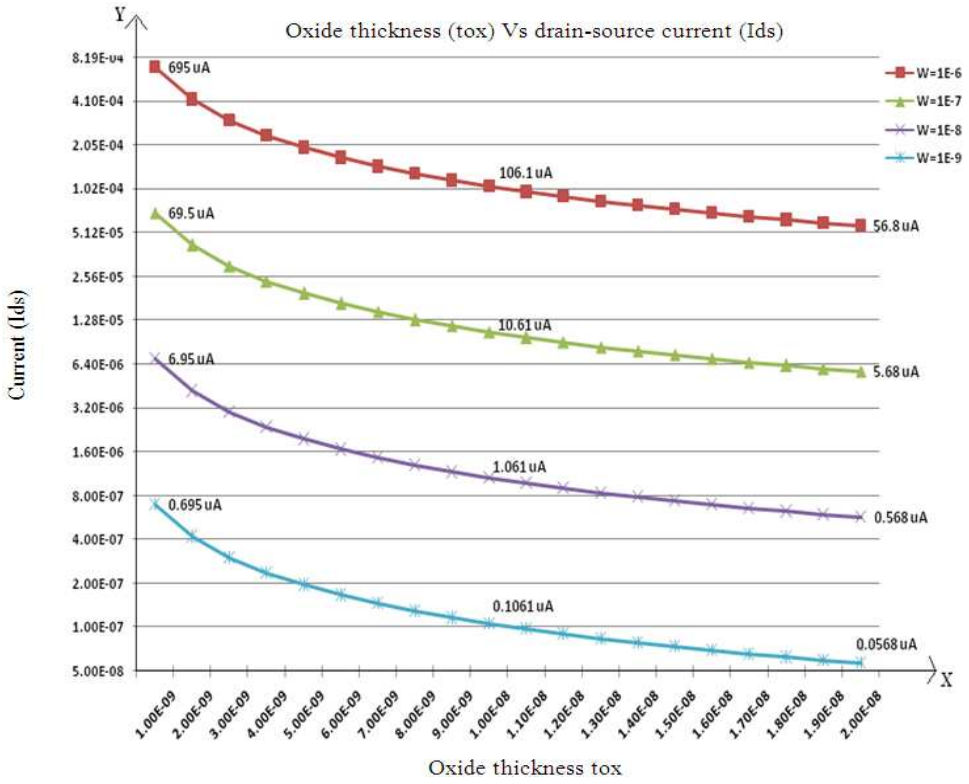

Fig. 6: Experimental graph results of varying gate oxide thickness and corresponding I_{ds}

- The Oxide thickness of the gate must be made adjustable
- It should satisfy the requirement of the device, which behaves as a multifunctional device
- It should be free from any interference

The other parameters like Gate, source and Drain Capacitances are made to vary favourably to make the device multifunctional. The equations relating to linear region and saturated region (2) and (3) respectively are modified as given below

Linear region:

$$I_{ds} = \frac{\varepsilon_{ox(new)}}{t_{ox(new)}}.\mu.\frac{W}{L}.\left[\left(v_{gs} - v_t\right).v_{ds} - \left(\frac{v_{ds}^2}{2}\right)\right] \quad (4)$$

Saturated region:

$$I_{ds} = \frac{\varepsilon_{ox(new)}}{t_{ox(new)}}\mu.\frac{W}{2L}.\left[\left(v_{gs} - v_t\right)^2\right] \quad (5)$$

where, $t_{ox(new)}$ refers to adjustable Gate Oxide thickness and it can vary as-ve integers.

Gate oxide thickness is the parameter which is physically variable and it should be adjusted on the basis of requirement to change the output current and not by adjusting the V_{gs}. This in turn defines the device to be operated at various I_{ds}. From Fig. 5 and 6, the following points are observed:

- Output characteristics remain unaltered for fixed $V_{gs,}$ but I_{ds} varies with change in the variable Gate oxide thickness t_{ox}
- Current varies from milliamps to micro amps and even to lower levels
- The simulation is ideal to prove that, even for the width at 1e-9, the above characteristics are realized with the change only in output current. It is important to note that V_{gs} is unaltered for all the output curves

The above Eq. 4 and Eq. 5 are modified based on the new material which is a new layer instead of SiO_2 layer.

Thermal effects: Another important aspect of simulation is that the device under consideration is supposed to operate at various current levels ranging from microamps to milliamps.

CONCLUSION

This study explains a concept based on simulation alone. It clearly indicates that if Gate oxide thickness of the Fig. 7a-f are demonstrates the simlation steps involved in fabrcating the new proposed device using microwind simulation, it gives both 2D and 3D view.

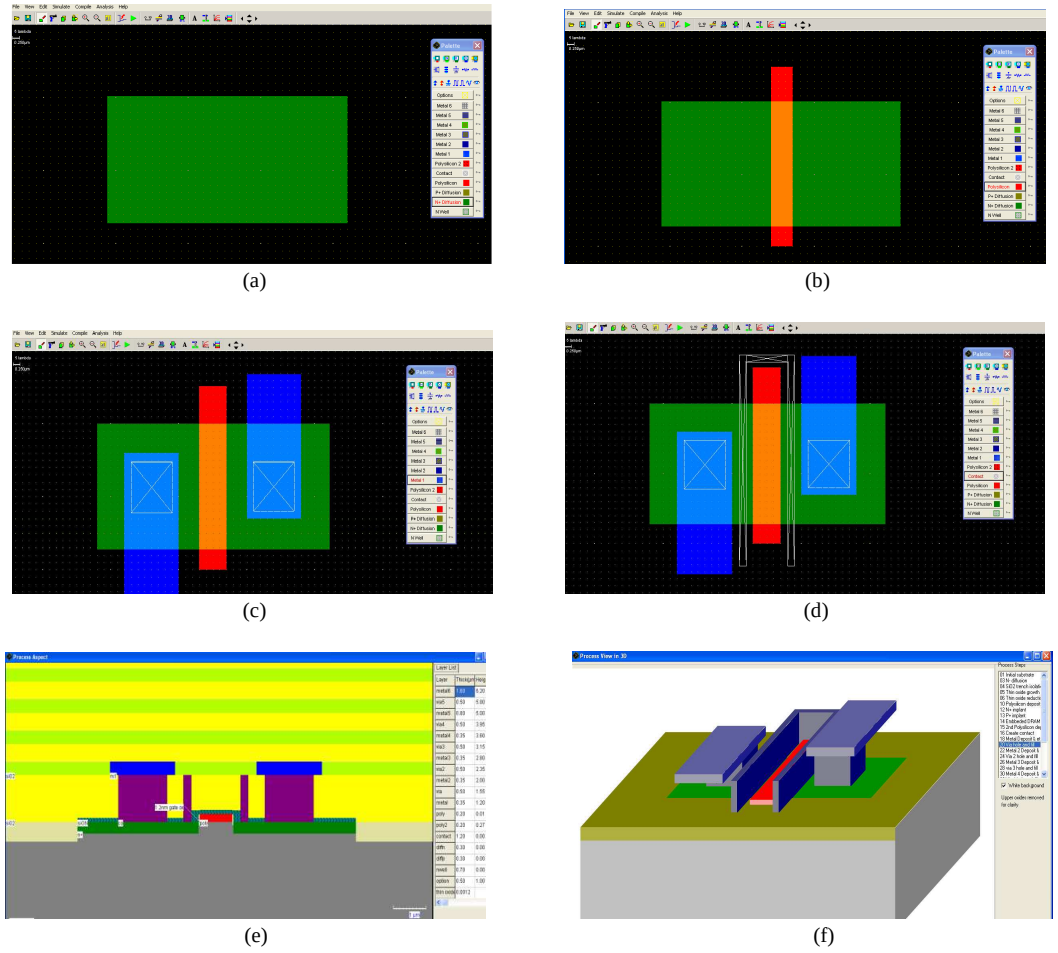

Fig. 7: (a) N+ Diffusion (b) Ploy Silicon (c) Contact with Metal (d) Proposed new device with externally controlled gate (e) 2D View (f) 3D View

In simple terms any conductor beyond its limits of carrying capacity should burn out. This simulation results depict the fact that current decreases from milliamps to microamps as the width is varied from micro level to nano level and below. It is observed that the Current I_{ds} vary with a decreasing trend. So the thermal effect may not have a huge variation. Here the idea is to have a single device for multiple output characteristics, which in turn performs multiple functions and reduces the number of devices that are required to construct a circuit.

A device is made to be adjustable, then the single device can exhibit multiple characteristics. This has to be accomplished by using a new technique which no way affects the device functionality and performance. The technology may be heterogeneous and one that combines mechanical concepts likes NEMS. It should be rihtly supported by the new type of material selection (Keller *et al*., 1999, Nakazato *et al*., 1993). So when implemented, the device performs as perceived by the simulation result. Here the Gate oxide thickness is alone discussed. Other parameters like Gate, Source and Drain Capacitances are also considered as variables, but the width variation is assumed to be constant. The concept may be further fine-tuned by varying the width. This may give new ideas for research.

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